

B450 AORUS ELITE V2

PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8628CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8 / A_VDDPS5	
21	ALC887 CODEC	
22	AUDIO JACK	
23	AUDIO LED	
24	POWER SEQUENCE , A_VDDP	
25	PWM IR3567	

[illegible]

Model Name:B450 AORUS ELITE V2

Component value change history

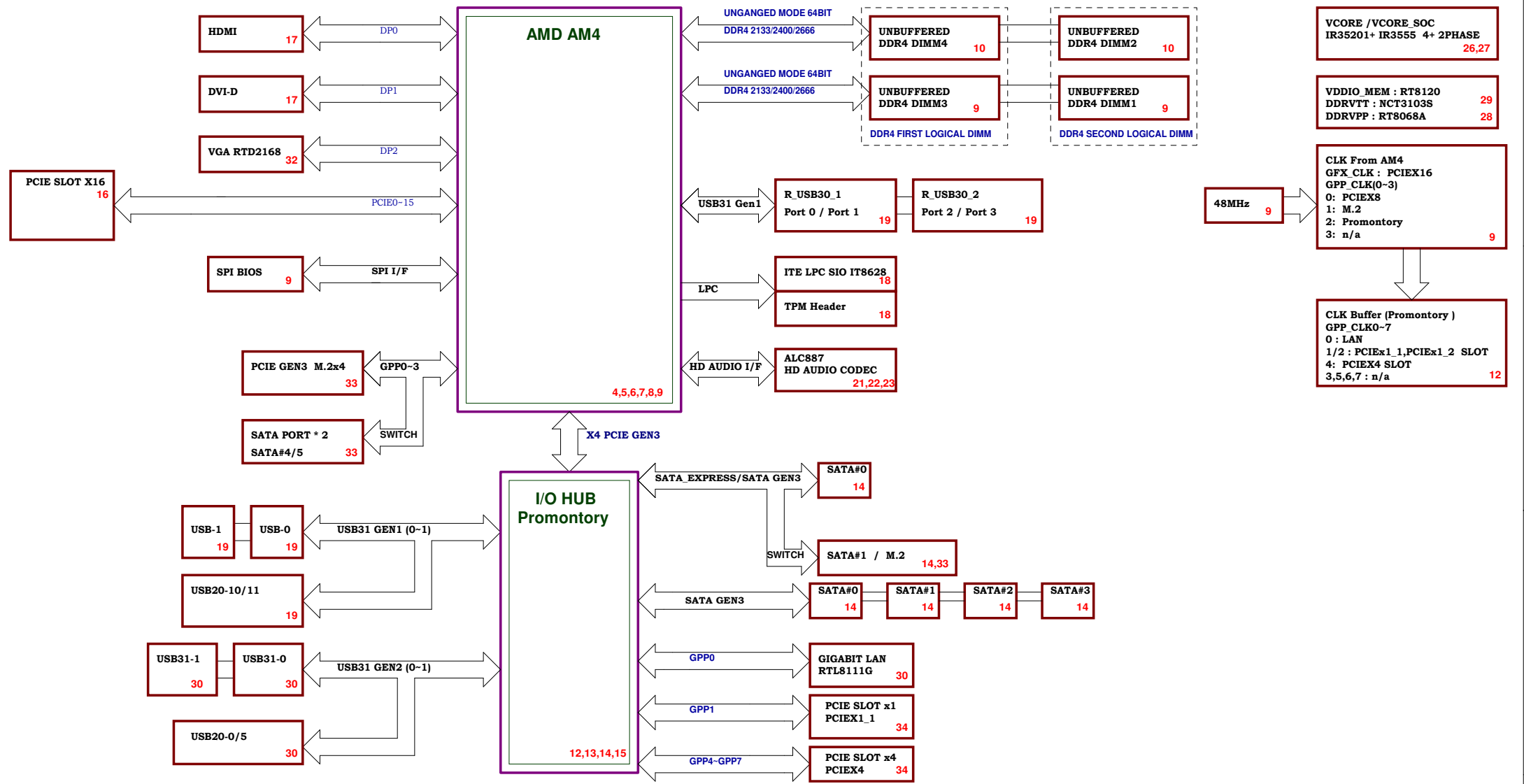
Version: 1.01

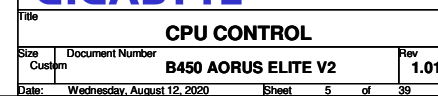
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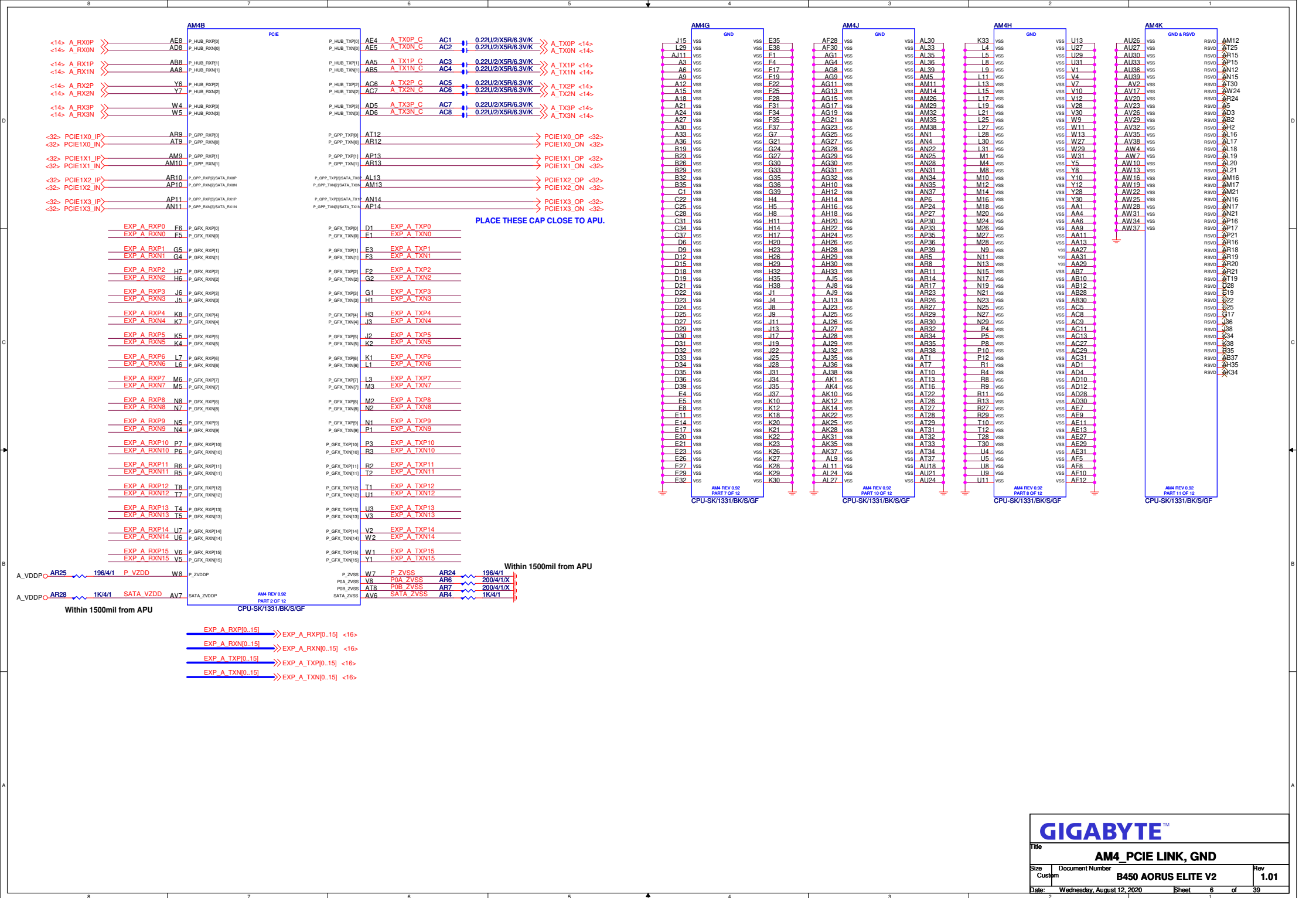
Date	Change Item		Reason
2017.02.23	10D P-BOM Release.	PCB: 1.0	1. AUDIO : 11CE2-651000-21R 2. NPEC1,EC31,EC24 : 11CO5-691000-11R /12R 3. 270U : 11CO5-8C2700-11R/12R 4. 560U : 11CO2-695600-21R/22R 5. HDMI : AZ1045-04F/MSOP10
2017.03.10			1. UPDATE EC FW TO V620.BIN
2017.04.27			1. UPDATE EC FW TO V622.BIN
2018.06.25	02 D-BOM Release.	PCB: 0.2	1. -MPD1 (LOCATION : FPESD) 2. LOCATION : PU6 pin30 原PE1_PRSNT- change to PE3_PRSNT- 3. location : M2BC17/M2BC13/M2BC18/M2BC19 請靠近m2b_socket 4. down size 0603 5. 新增裝甲 6. modify from B450 AORUS to B450 AORUS ELITE
2018.07.12	10 P-BOM Release.	PCB: 1.0	1. ECR50 for FAN_0 RPM PULL UP 2. MAR6/AR52/AR47/PR8 change to short-pad 3. KB_MS_USB 用料限制用-14R用料
2018.07.12	10B F-BOM Release.	PCB: 1.0	1. 修改ATX connect 用料:9I高溫料 [11NH4-020024-Z1R_11NH4-020024-Z2R]
2018.08.20	10G D-BOM Release.	PCB:1.01	1. Vcore SENSE 位置 2. C125 10u change to 22u 3. VINA0 change to APU_PWRGD(for summit / Pinnacle 不上DIMM時,僅亮CPU DEBUD LED,應改為亮DDR DEBUD LED) 4. BRN1 change to 1K
2018.09.21	10G SKIP PVTRelease.	PCB:1.01	SKIP PVT
2019.05.21	10H SKIP PVTRelease.	PCB:1.01	1. UPDATE NEW EC FW V684.BIN
2019.07.08	10H ECN	PCB:1.01	1. Location :AIO_SHIELD 11AIO-0C0013-02R 加管料11AIO-0C0013-12R
2019.11.12	10M ECN	PCB:1.05	1. Vcore choke Footprint 自動插件修改
2020.06.22	10L ECN	PCB:1.05	1. 新增替代料 - IT8795 (10HP2-118795-10R) , 統一使用 IT8795 以利後續備料
2020.06.22	10P MP	PCB:1.05	1. SIO CX-->DX(10HP2-118686-40R) 2. BOM : 9MB45ARSE-00-10P(與10L並存)
2020.07.23	10A EVT	PCB:1.0	1. CHANGE PWM 2. SOC CHOKE CHANGR 11LC5-M5300C-01C 3. BOM : 9MB45AET2-00-10A
2020.08.04	10B PVT	PCB:1.01	1. DR19-->3.83K, DR46/DR47-->3.09K, DR16-->3.32K, DR44/DR45-->22K 2. Location: DU1 -->10TA1-63567B-07R 3. 3. BOM : 9MB45AET2-00-10B
2020.08.04	10B ECN	PCB:1.01	1. Location:DEL1,DFL1 新增11LC5-F5300C-08R自動插件料號

Circuit or PCB layout change for next version

[illegible]

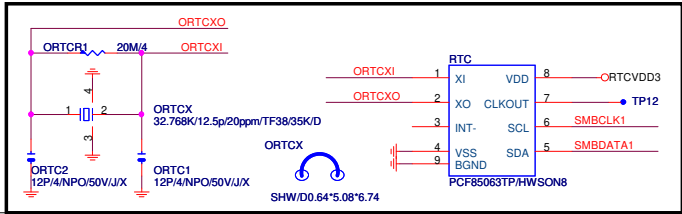




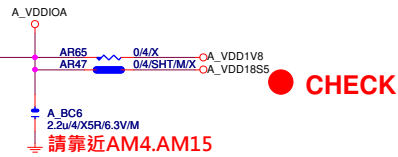
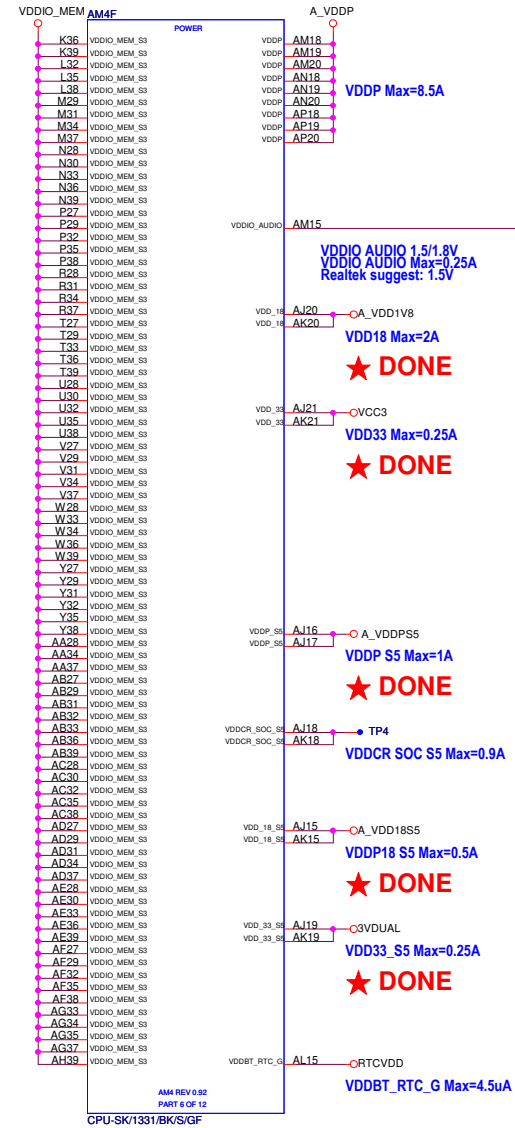


TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 480kHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 480kHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 1000kHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic (DEFAULT)	Coin battery is not on board.	LPC ROM	short reset mode	Use 1000kHz PCIE clock as reference clock and generate internal clocks only
C3/ST DIE ONLY							ZP DIE ONLY



GIGABYTE™			
Title			
AM4 MISC			
Size	Document Number	Rev	
Custom	B450 AORUS ELITE V2	1.01	
Date:	Wednesday, August 12, 2020	Sheet	7 of 39



● CHECK

VDD18 Max=2A

★ **DONE**

VDD33 Max=0.25A

★ DONE

④ A VDDPSE

VDDP S5 Max=1A

• **TD4**

VDDCR SOC S5 Max=0.9A

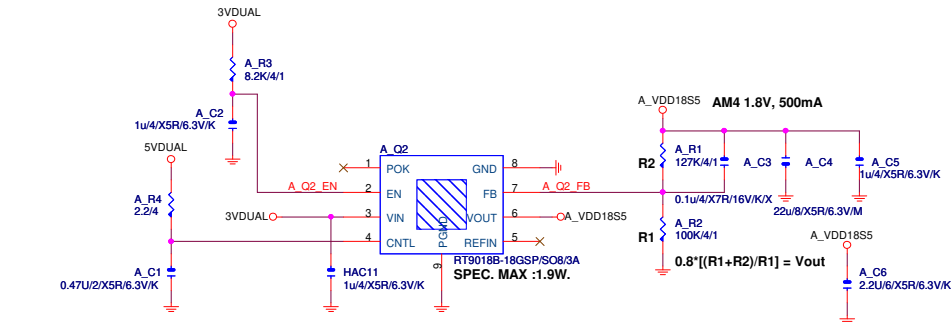
VDDP18 S5 Max=0

100

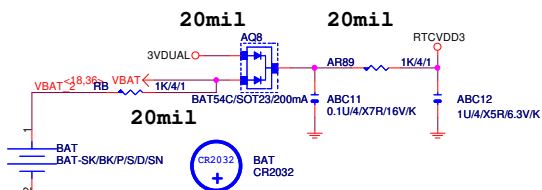
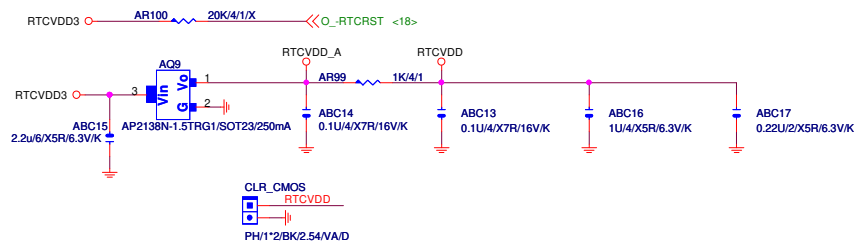
3VDUAL
VDD33 S5 Max=0.25A

★ **Done**

VDDBI_RTC_G Max=4.50uA



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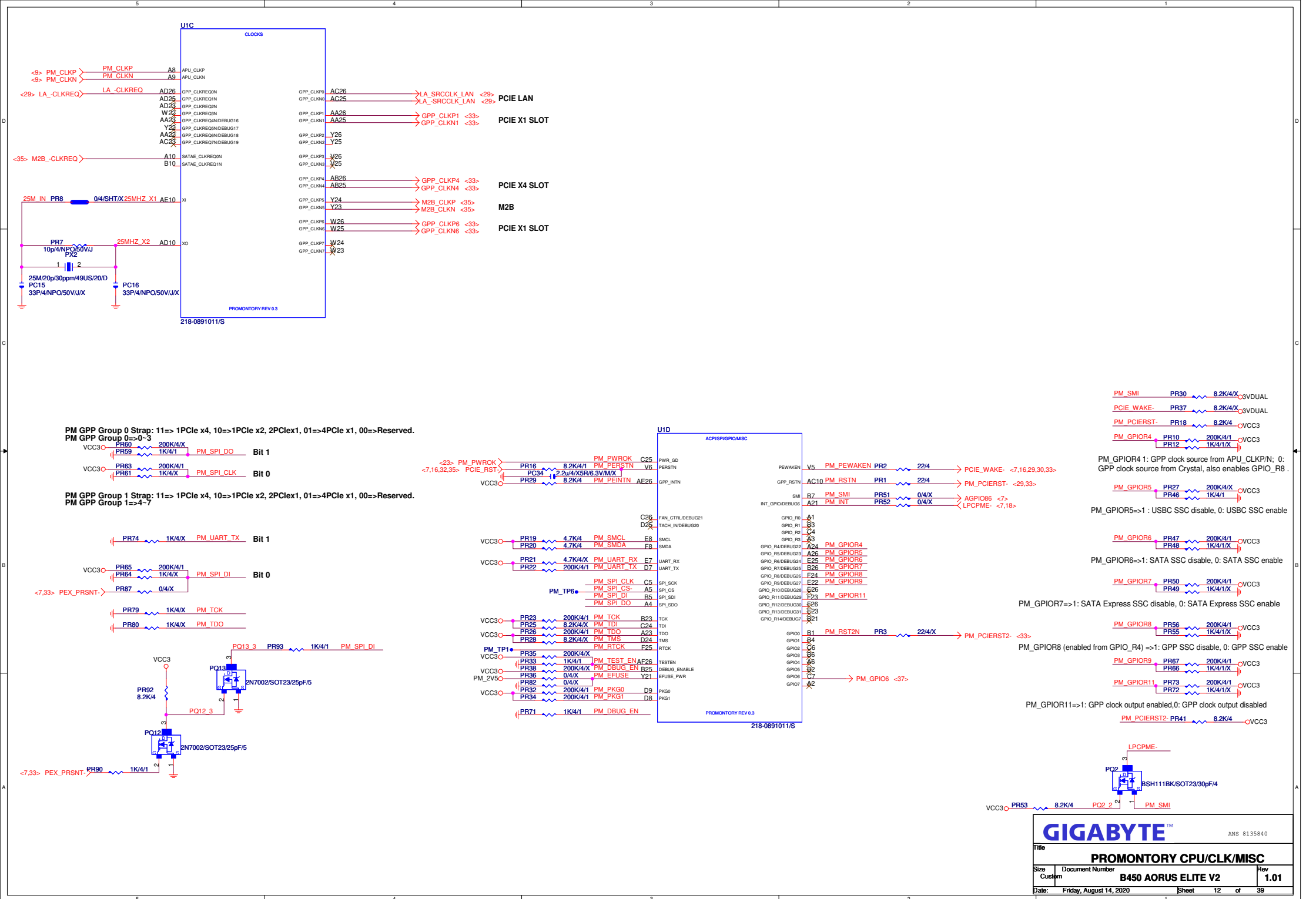
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

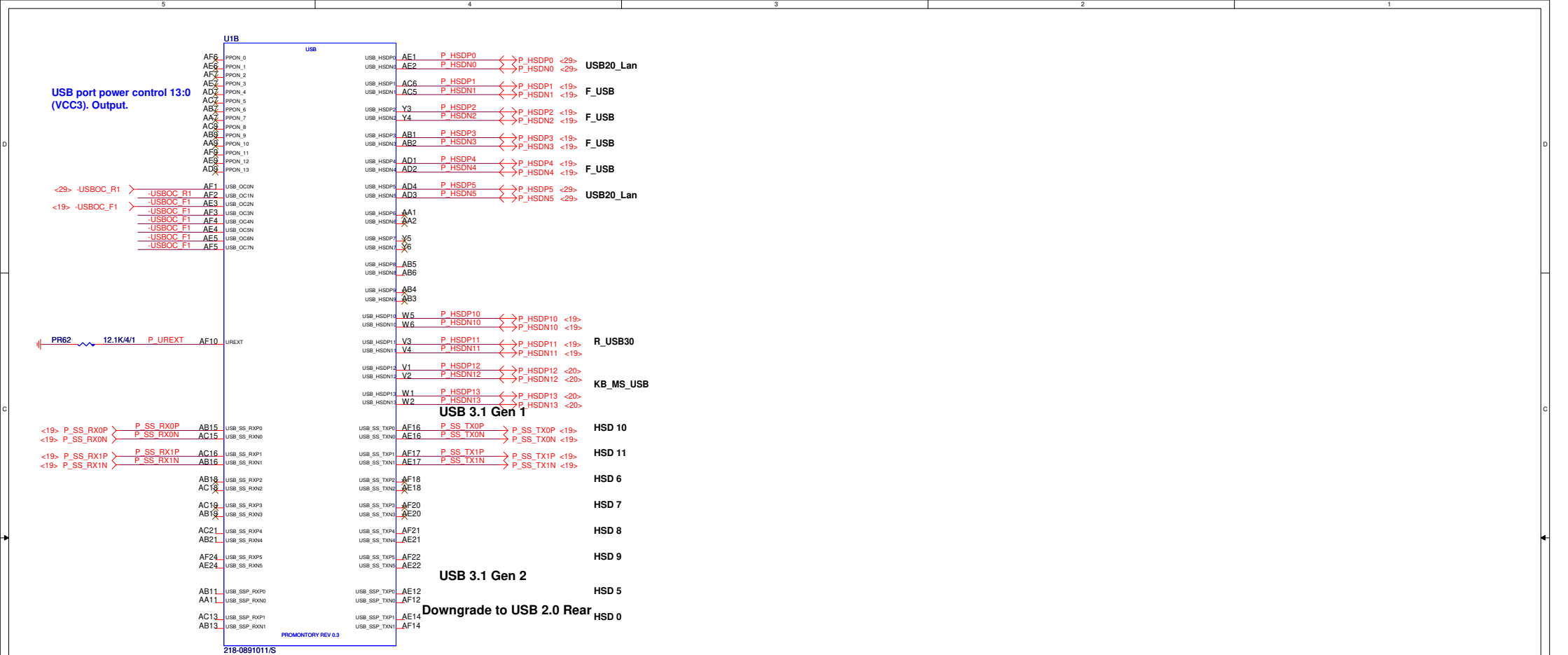
NOT ADD ICT FOR RTCVDD PIN



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GIGABYTE			
DDR4 CHANNEL B			
File	Document Number	B450 AORUS ELITE V2	
Size	Count	1.01	
Wednesday, August 12, 2020			

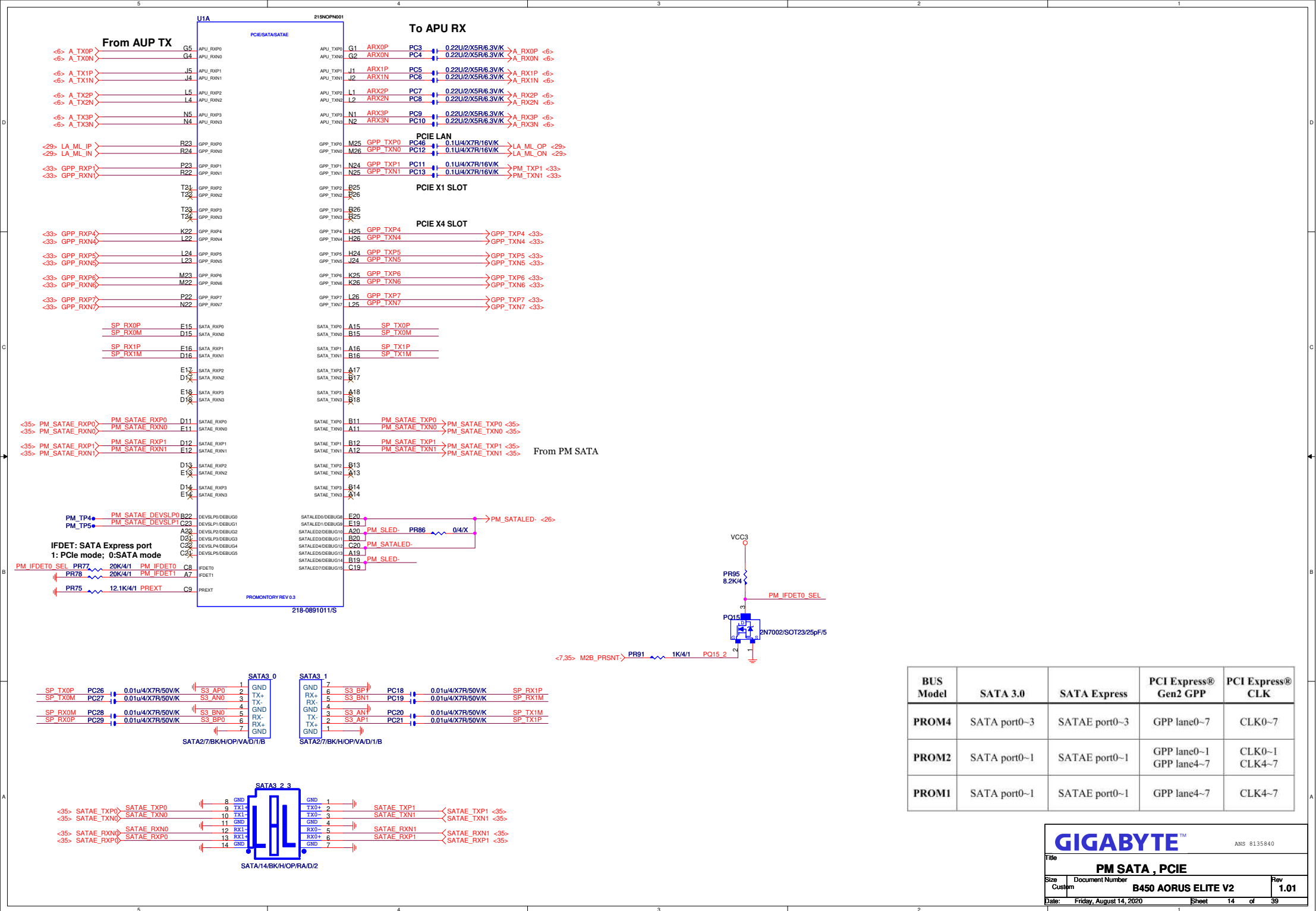


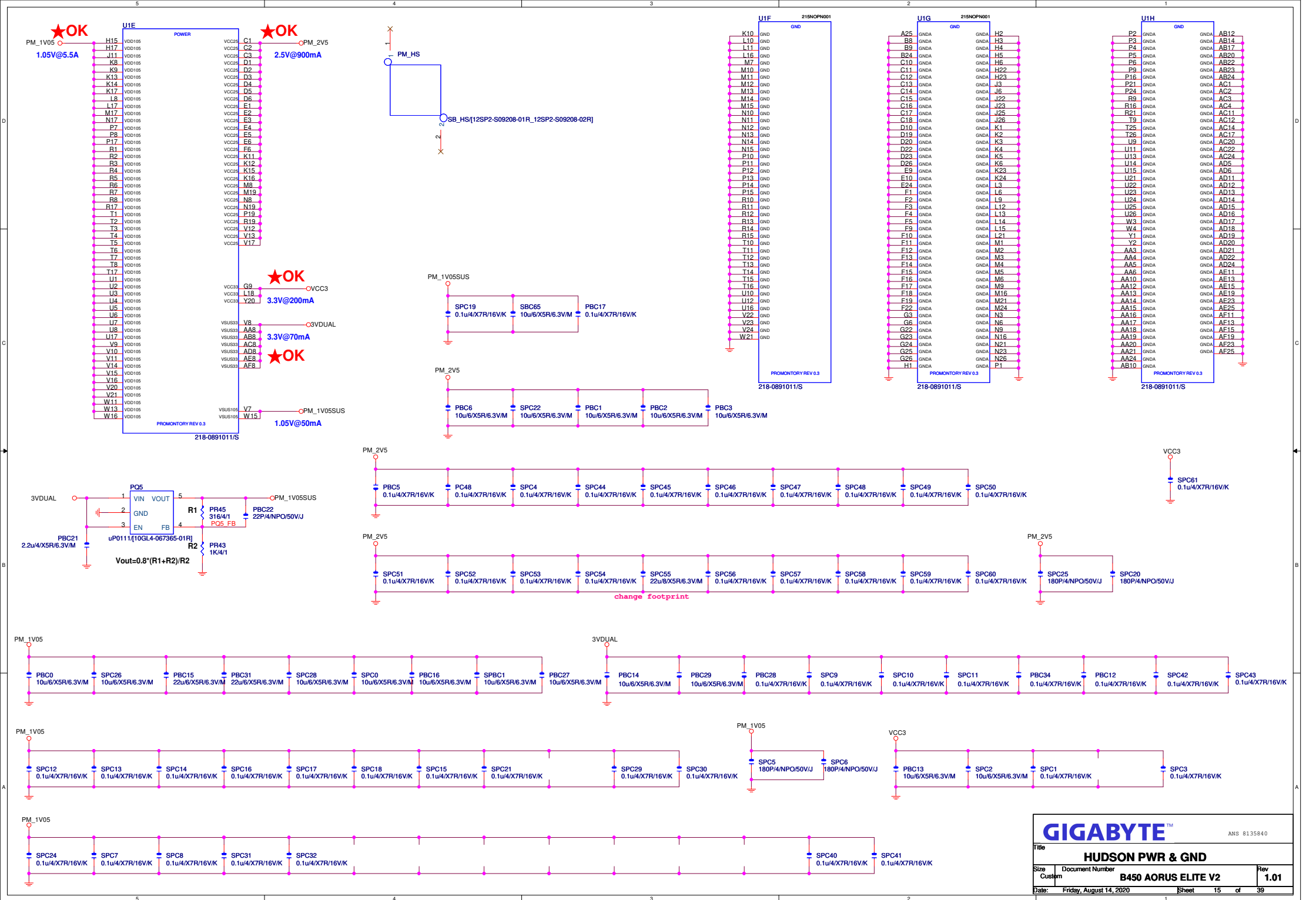


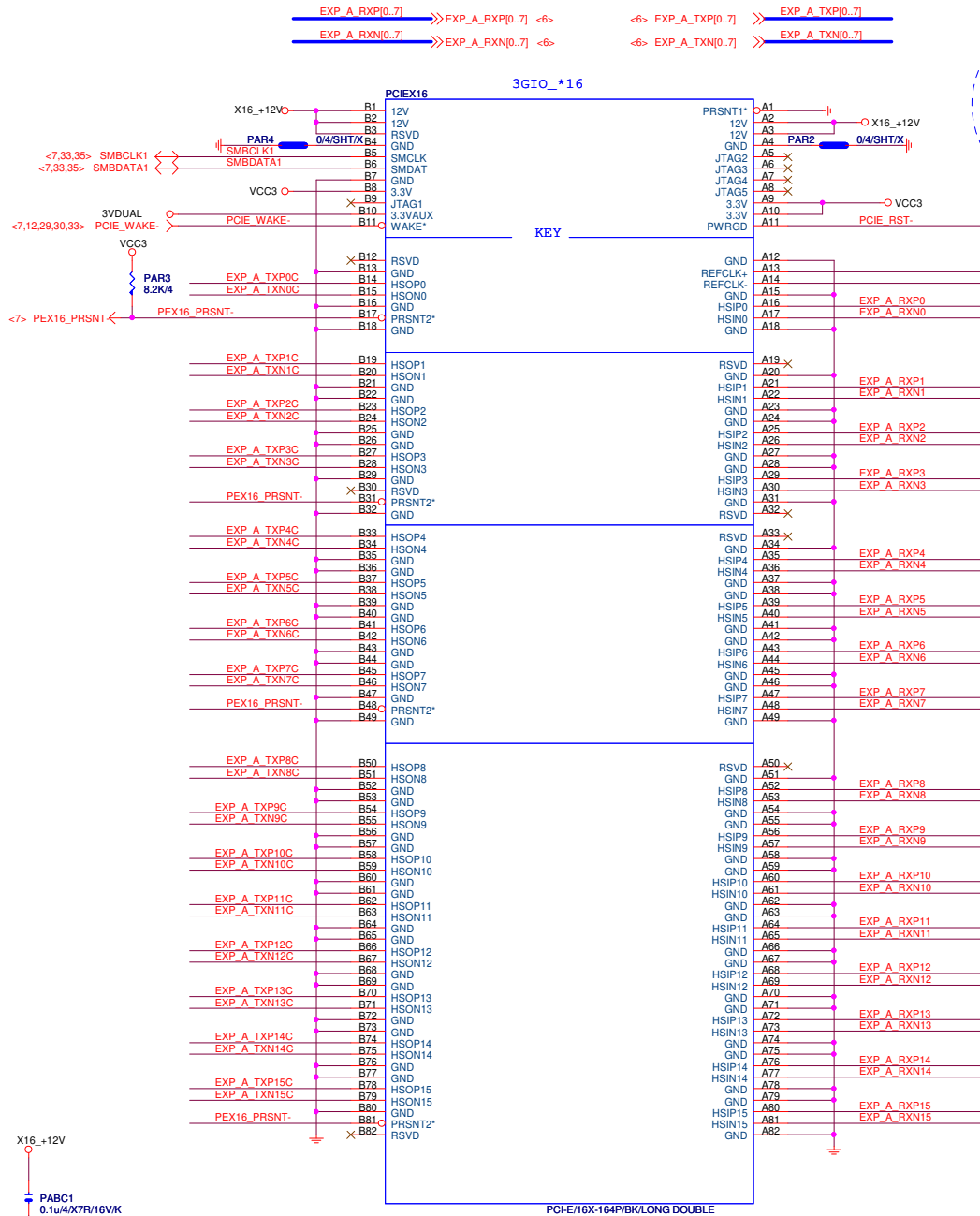
USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

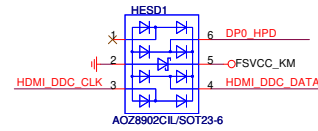
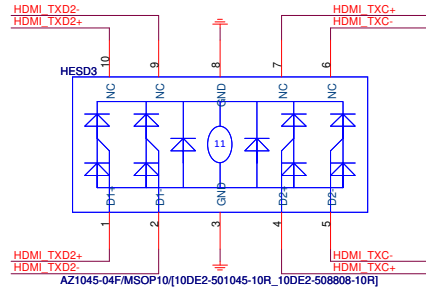
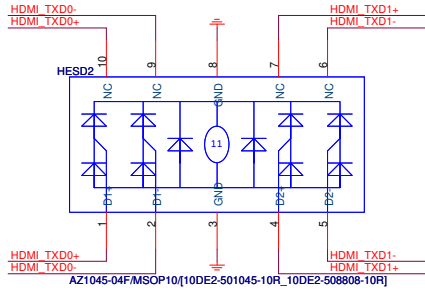
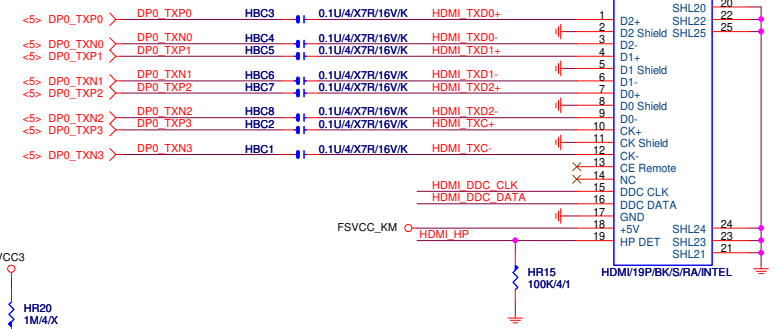
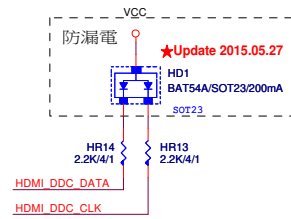
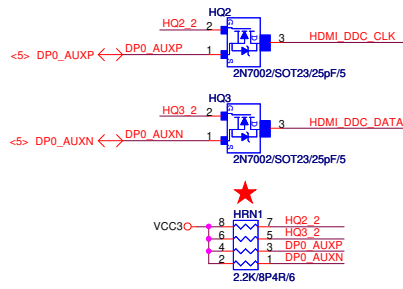
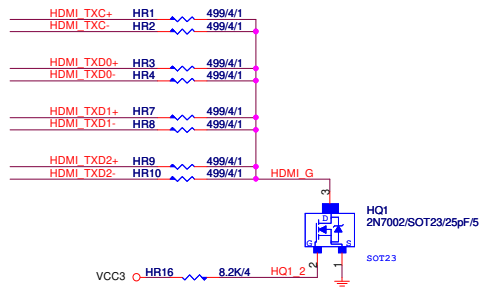
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

		ANS 8135840
Title		
PM USB		
Size Custom	Document Number <div style="text-align: center; font-weight: bold; font-size: 1.2em;">B450 AORUS ELITE V2</div>	Rev <div style="text-align: center; font-weight: bold; font-size: 1.2em;">1.01</div>
Date: Friday, August 14, 2020		
Sheet 13 of 39		





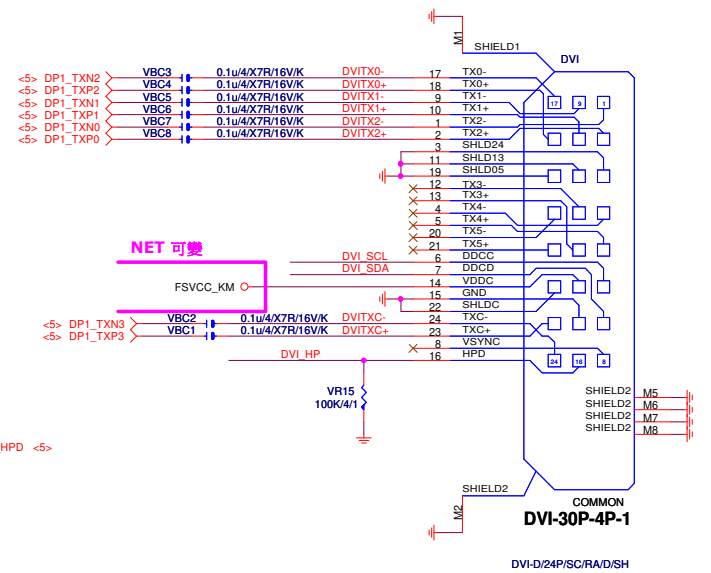
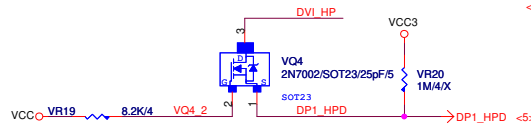
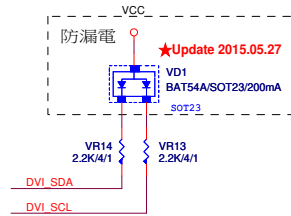
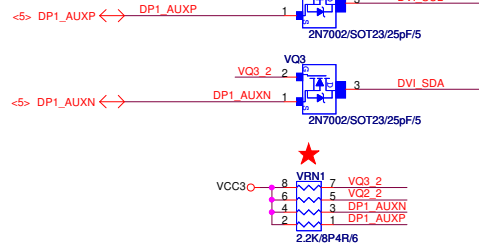
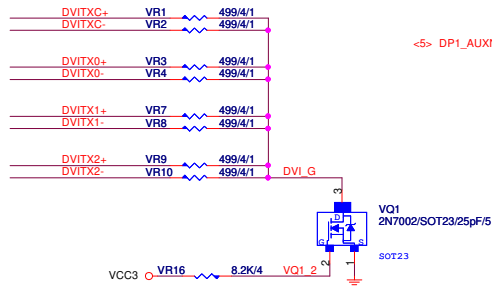




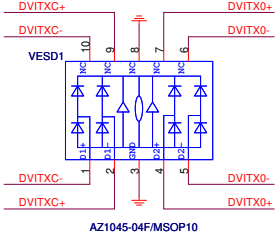
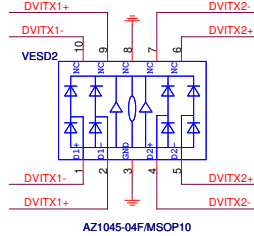
Rev: 0.73

DVI CONN

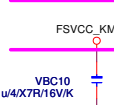
DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



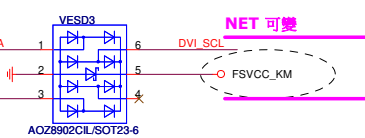
Close to connector



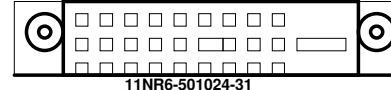
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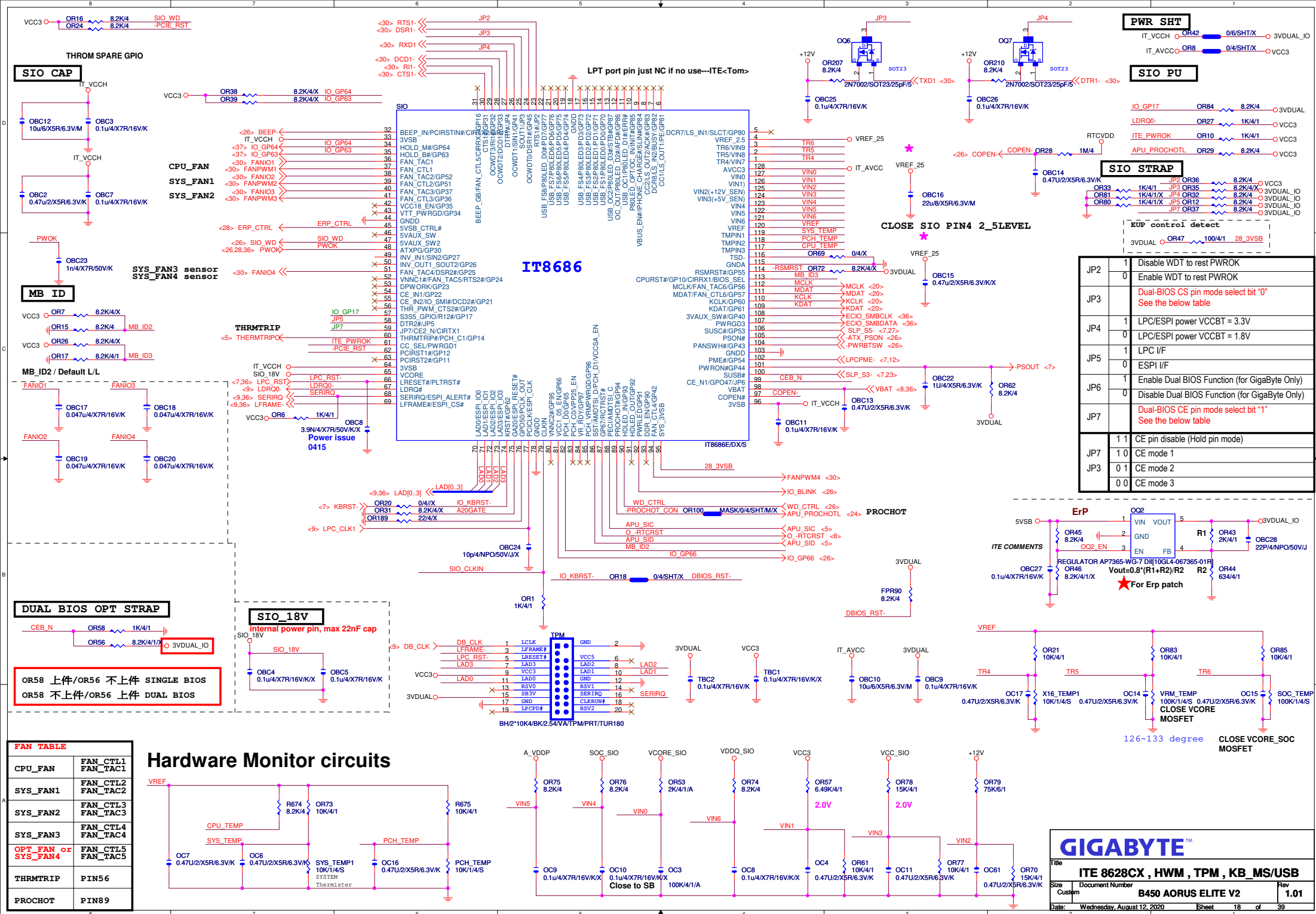
Close to connector



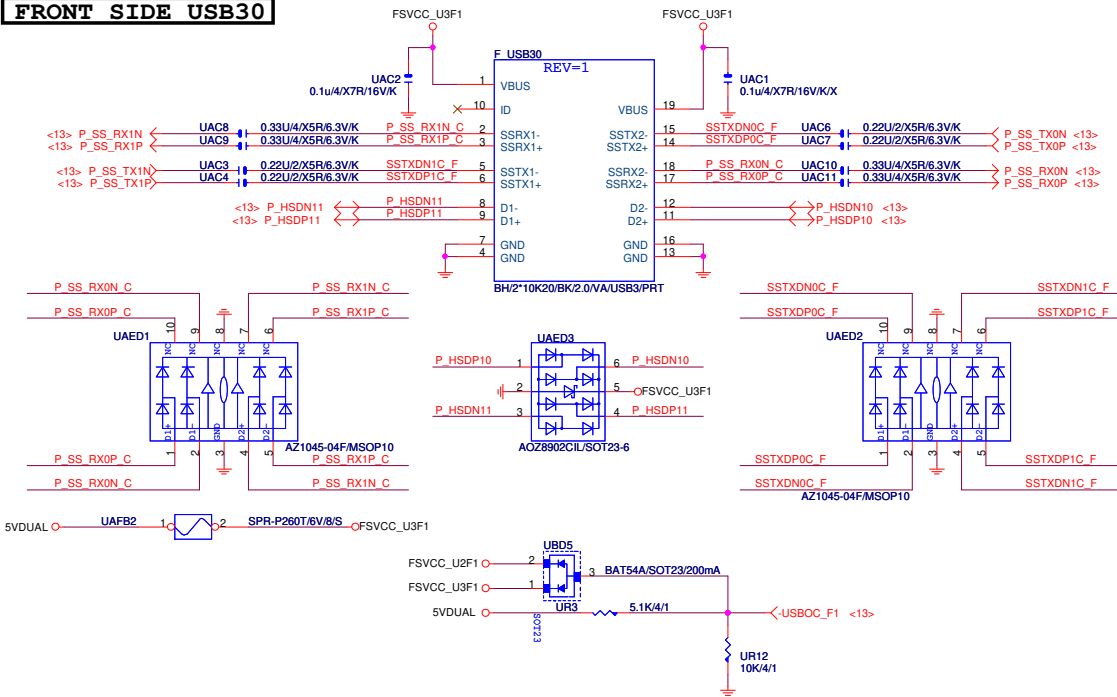
平躺式 DVI-D



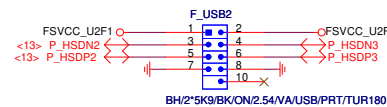
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HDMI 2.0		
Title	Document Number	Rev
Size	B450 AORUS ELITE V2	1.01
Date:	Wednesday, August 12, 2020	Sheet 17 of 39



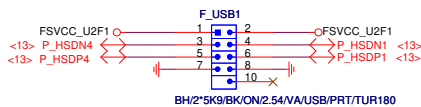
FRONT SIDE USB30



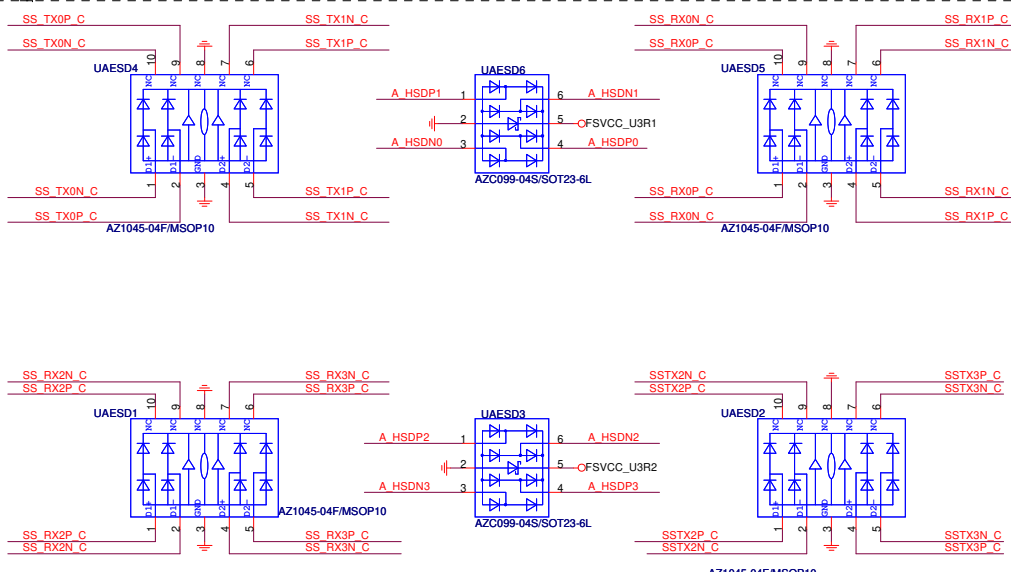
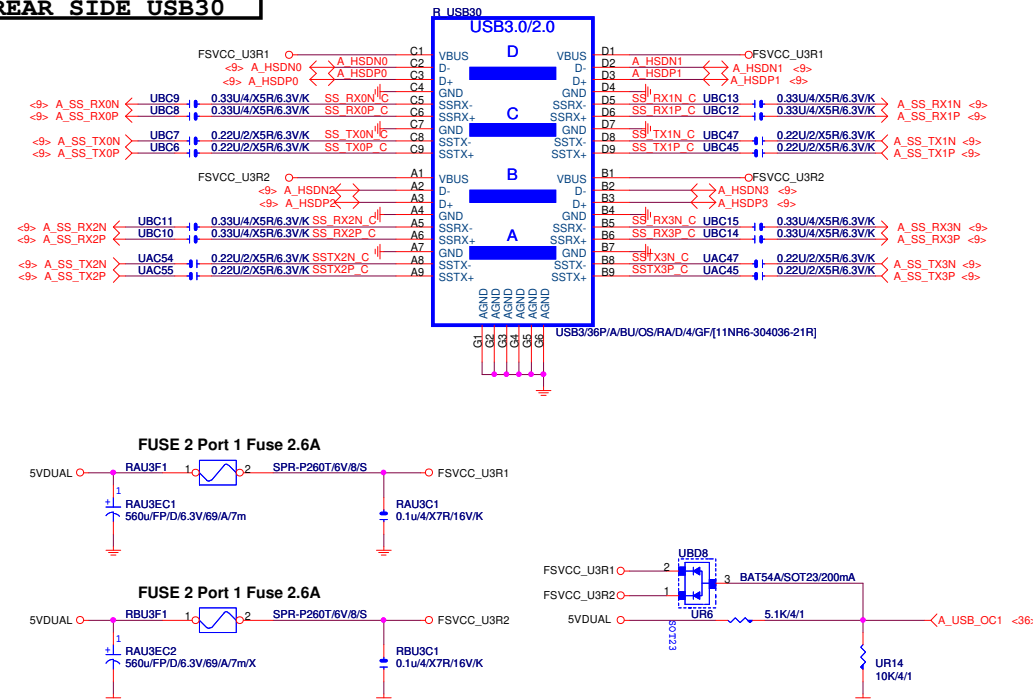
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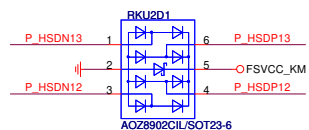


FRONT SIDE USB1

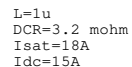


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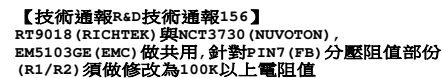




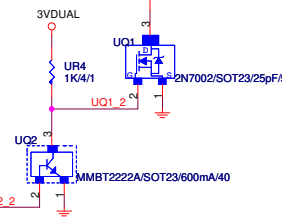
A VDD1V8



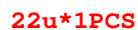
CHOKES與CAP料號可變



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V



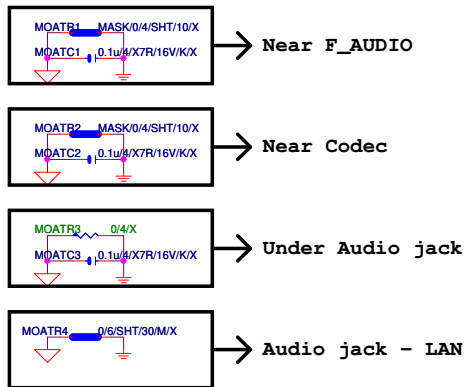
<5,23,36> CORETYPE1



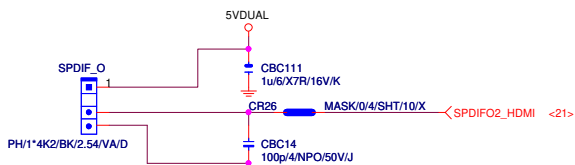
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Title			
FAN, A_VDD1V8			
Size	Document Number	Rev	
Custom	B450 AORUS ELITE V2	1.01	
Date:	Wednesday, August 12, 2020	Sheet	20 of 39

Rev 3.0

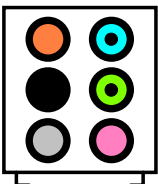


*量産前, 0ohm改short pad



For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK

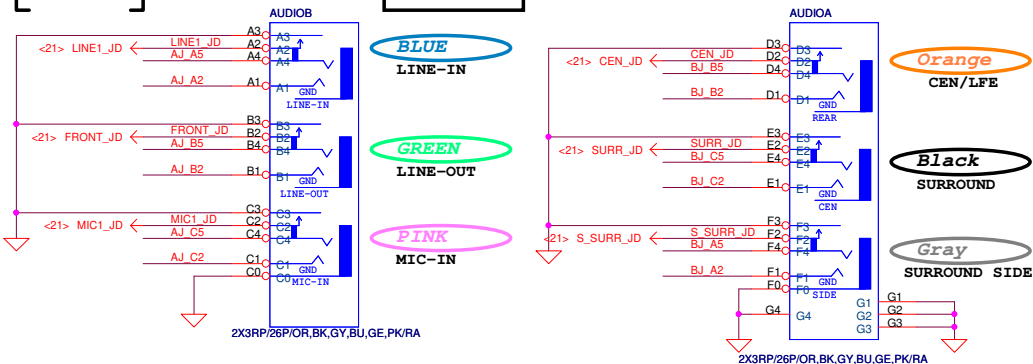


AZALIA JACK

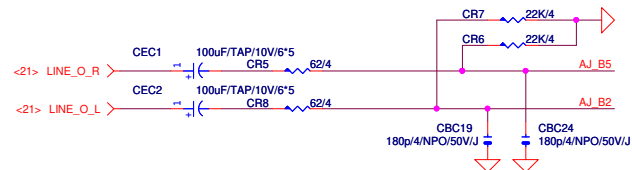
BLUE
LINE-IN

GREEN
LINE-OUT

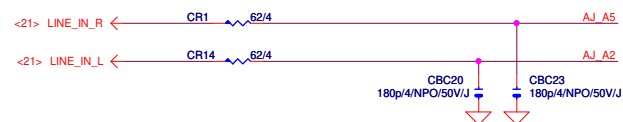
PINK
MIC-IN



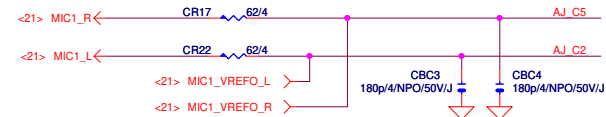
LINE-OUT



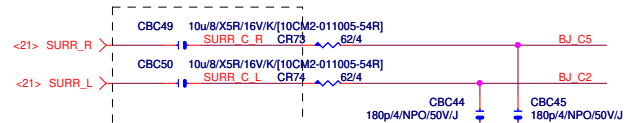
LINE-IN



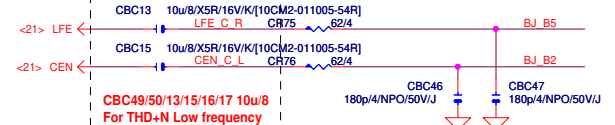
MIC-IN



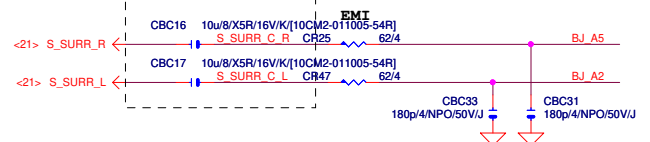
SURROUND



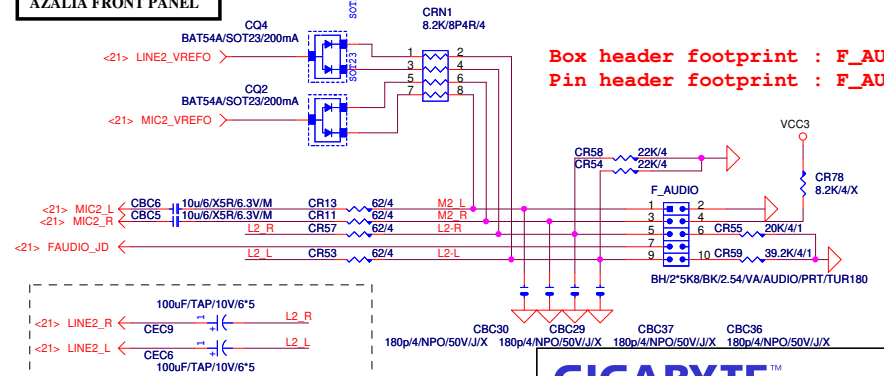
CEN/LFE



SURR BACK



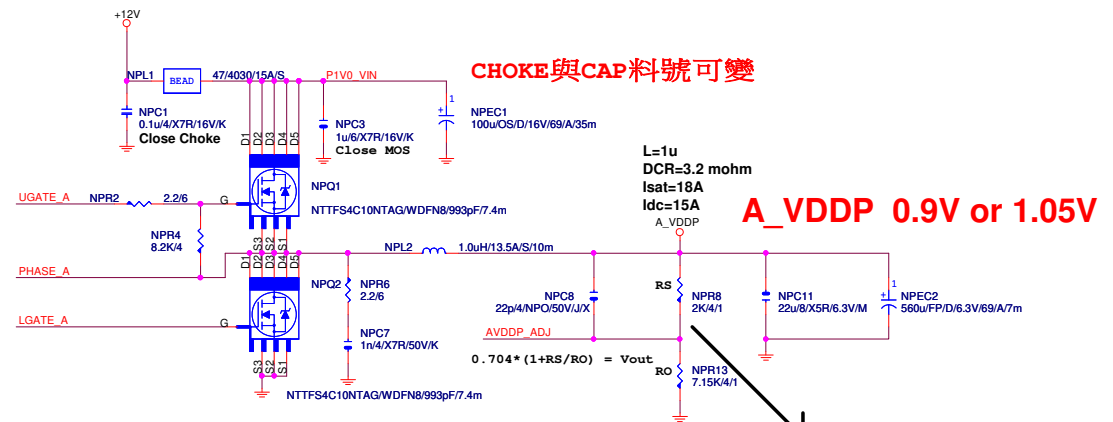
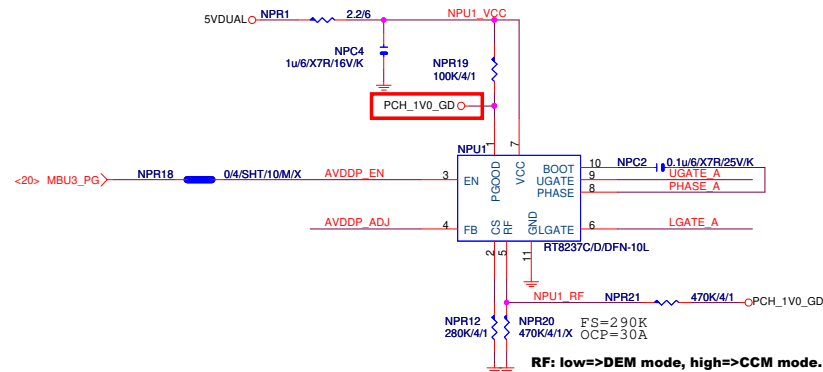
AZALIA FRONT PANEL



Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S

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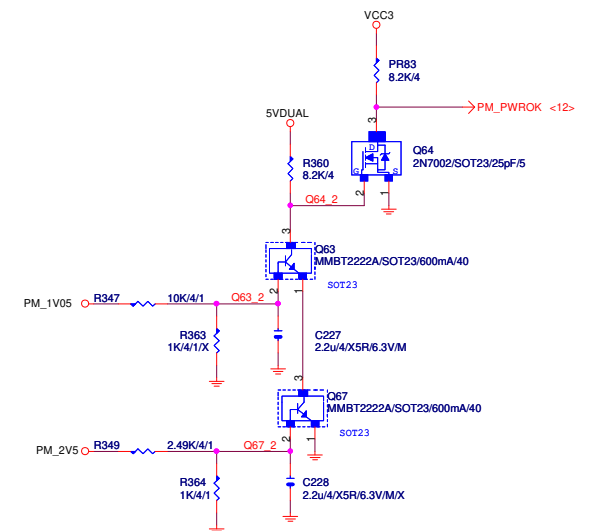
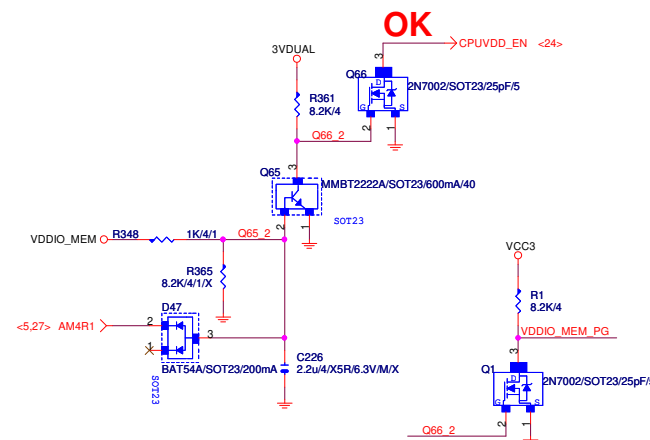
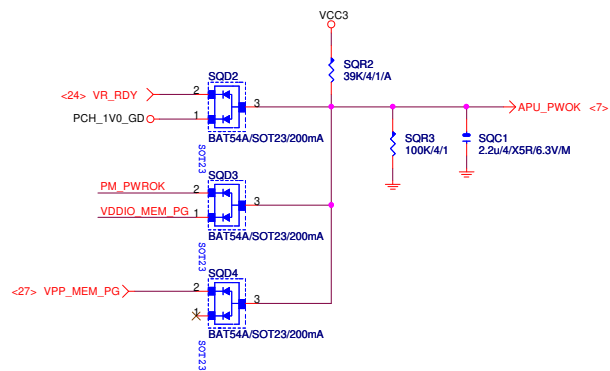
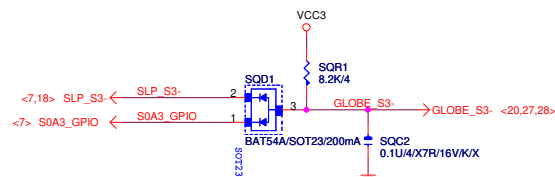
Title			AUDIO JACK
Size			Document Number
Custom			B450 AORUS ELITE V2
Date:			Wednesday, August 12, 2020
Sheet			22 of 39
Rev			1.01



請放置CHOKES—出來的地方

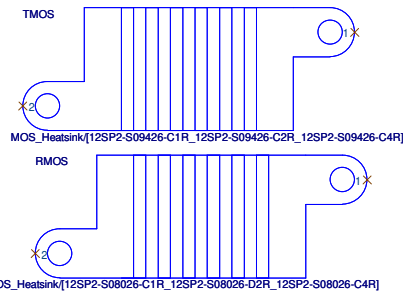
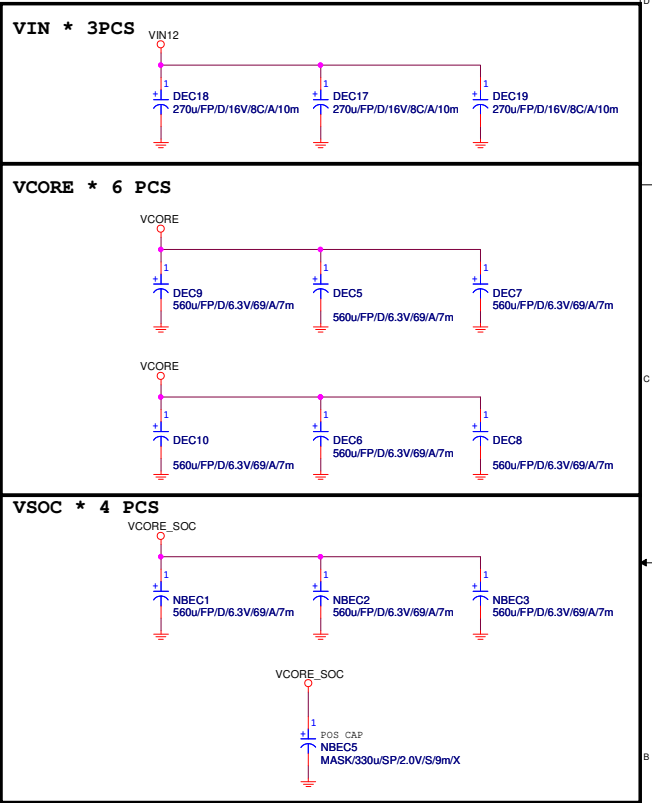
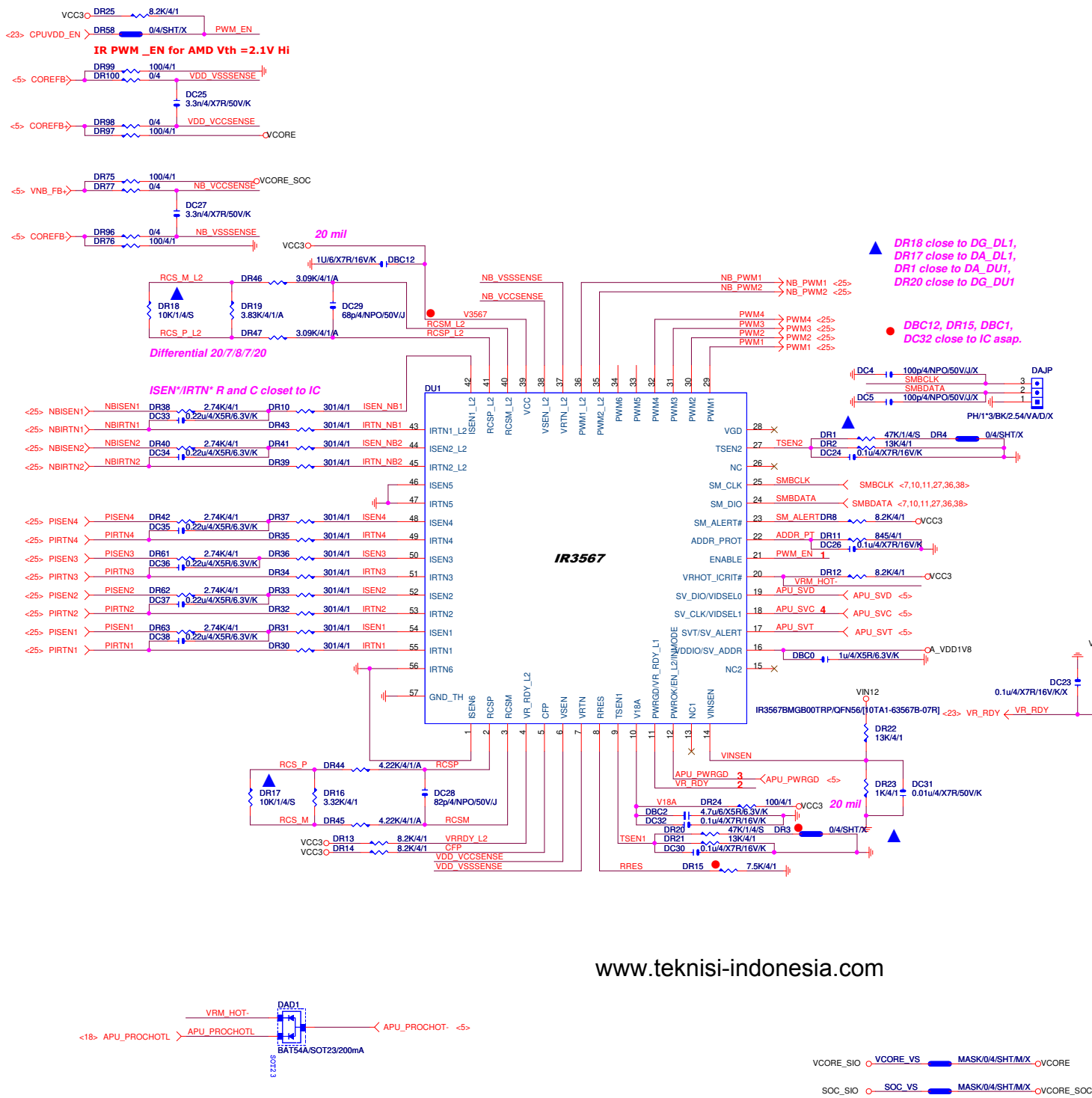
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

Remote sense請從最重的負載端點拉回



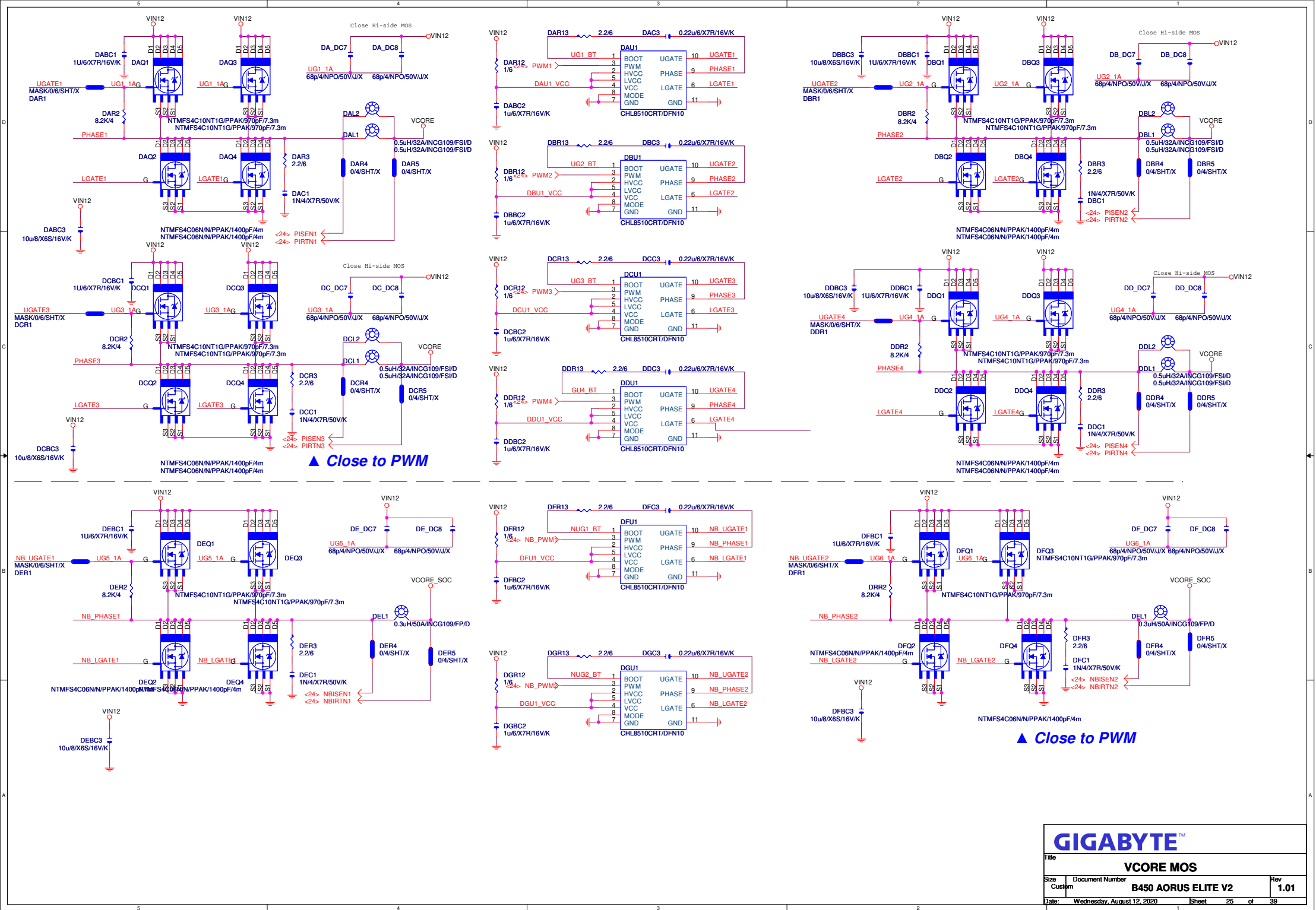
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POWER SEQUENCE		
Title	Document Number	Rev
Size	Custom	1.01
Date:	Wednesday, August 12, 2020	Sheet 23 of 39



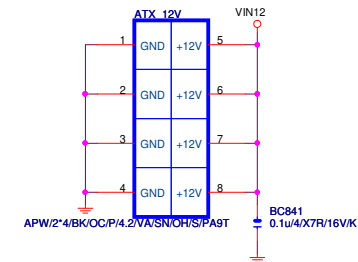
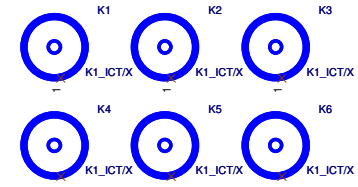
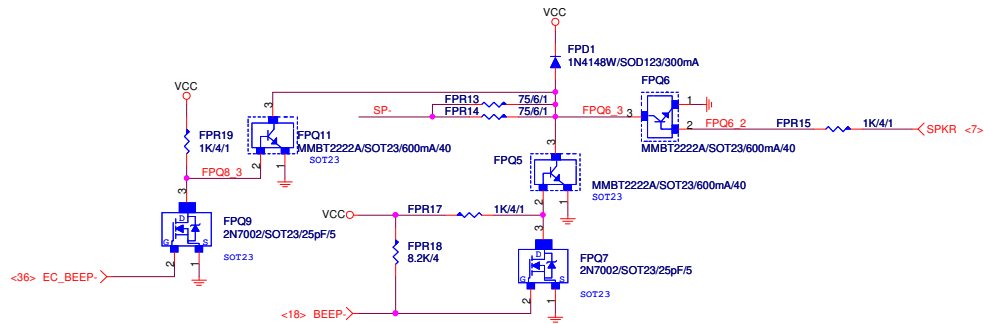
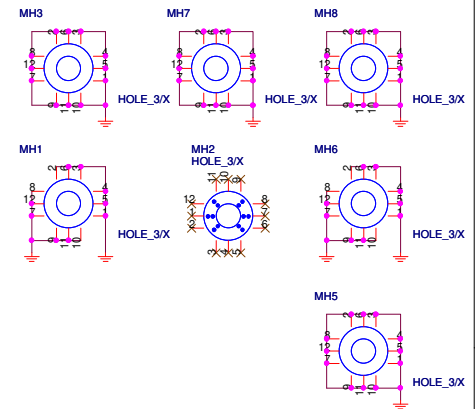
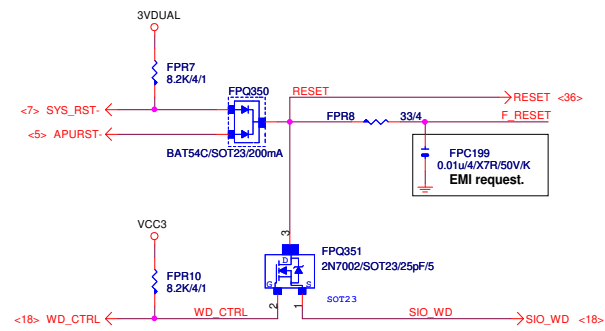
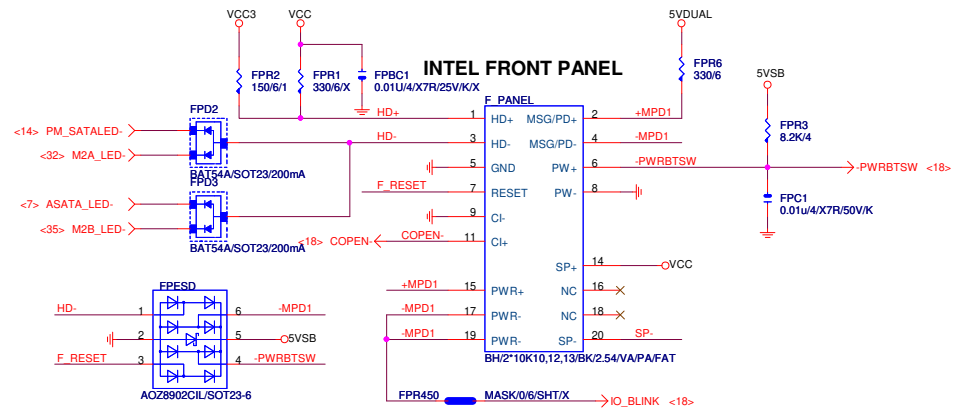
GIGABYTE
Title
VCORE (PWM ISL6277+6609A)
Size Custom
Document Number
B450 AORUS ELITE V2
Date: Wednesday, August 12, 2020
Rev
1.01
Sheet
24
of
39

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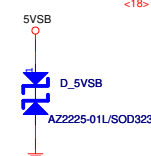
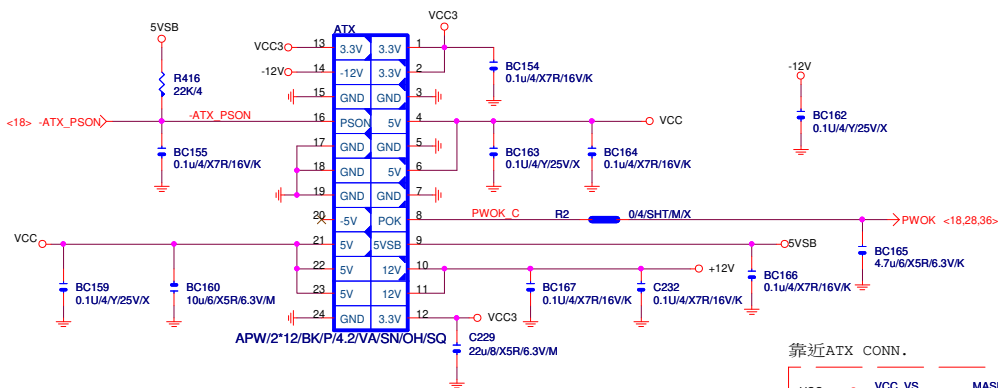


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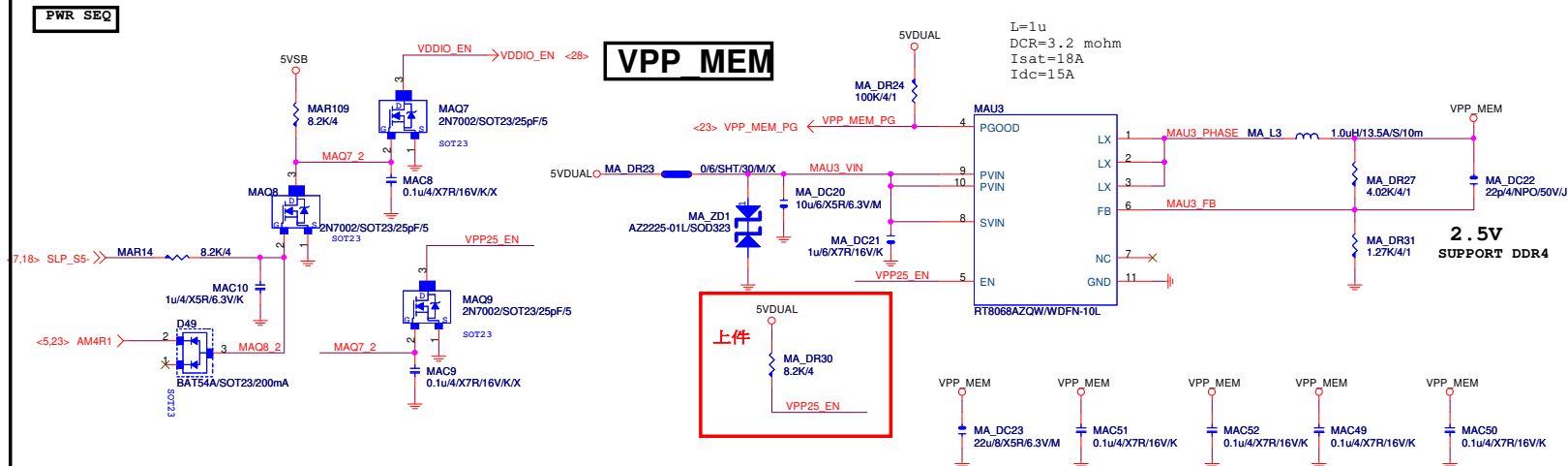
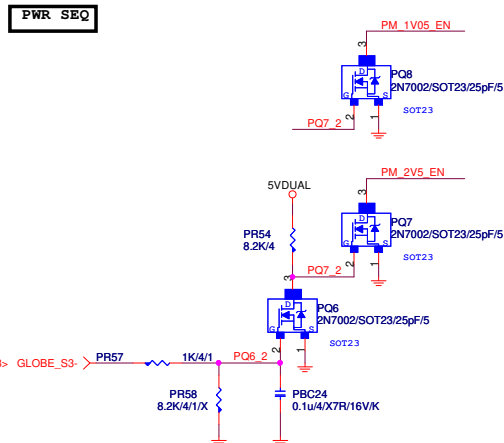
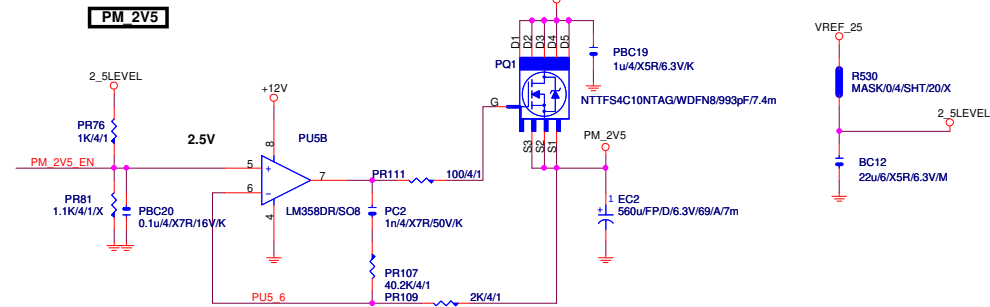
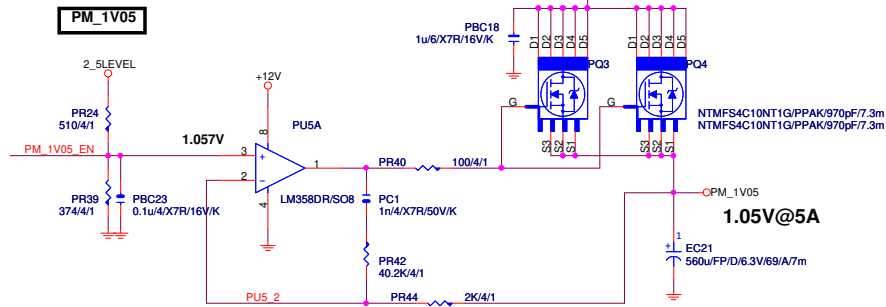
Title			VCore MOS
Size	Document Number	Rev	
Custom	B450 AORUS ELITE V2	1.01	
Date:	Wednesday, August 12, 2020	Sheet	25 of 39



ATX POWER CONNECTOR



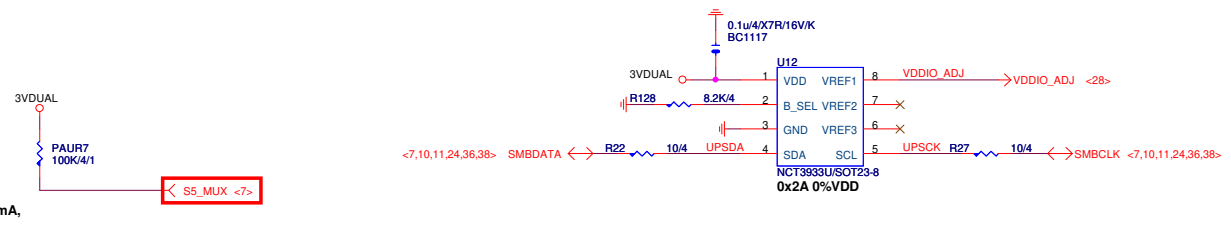
GIGABYTE™			
ATX, FRONT PANEL			
Title	Document Number	Rev	1.01
Size	Custom	B450 AORUS ELITE V2	
Date:	Wednesday, August 12, 2020	Sheet	26 of 39



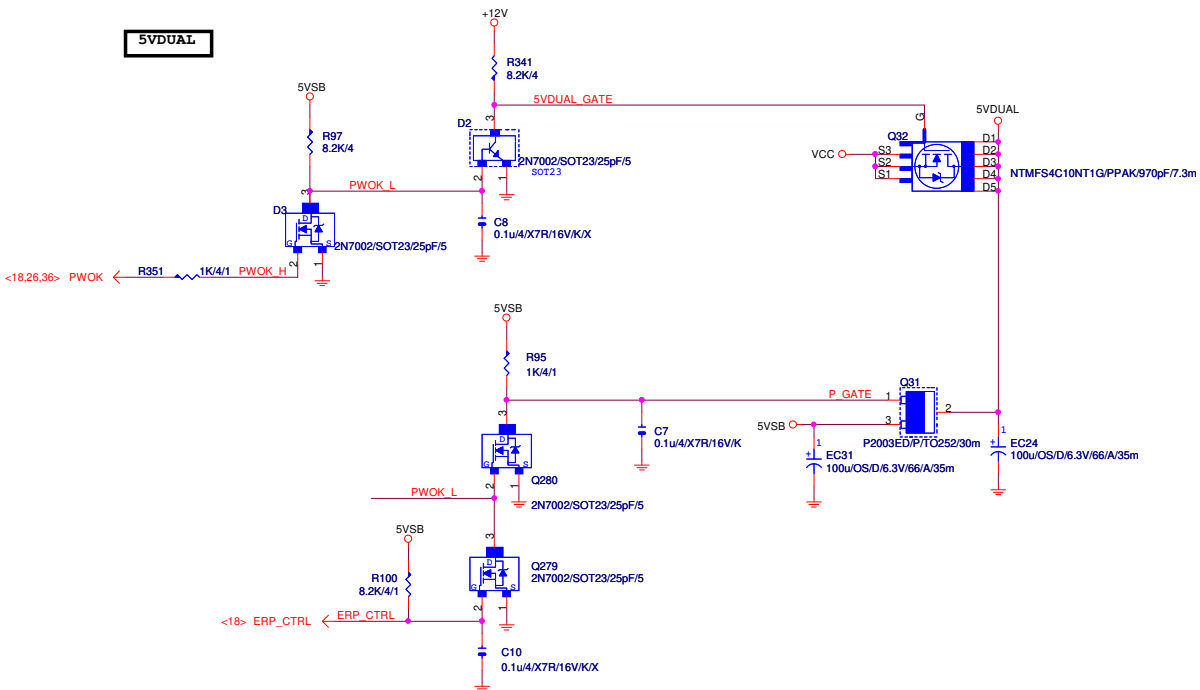
VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.

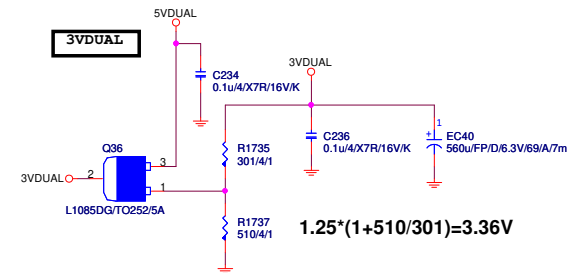
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5VDUAL

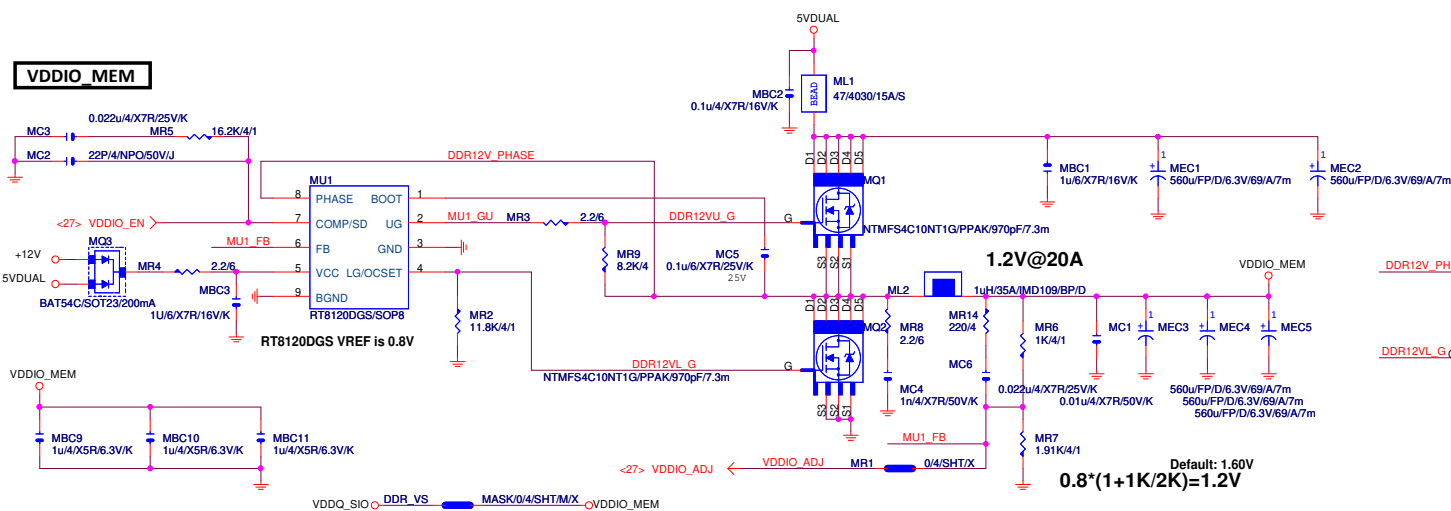


3VDUAL

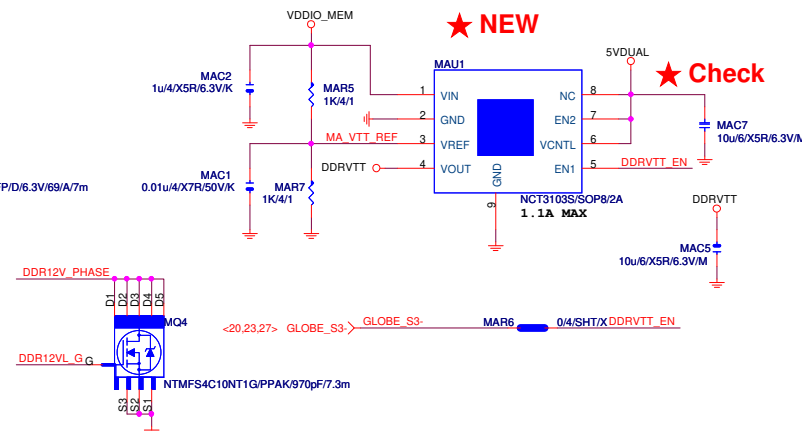


$$1.25 \times (1 + 510/301) = 3.36V$$

VDDIO_MEM

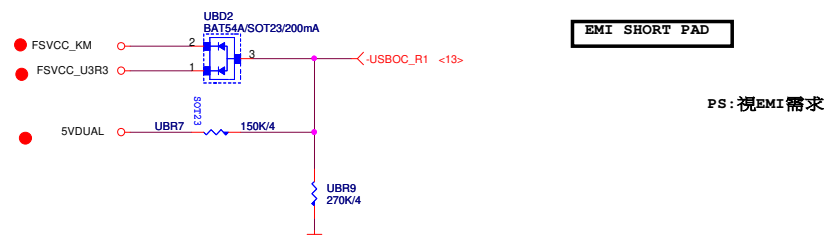
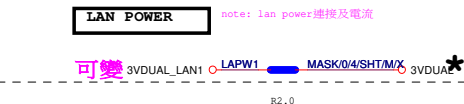
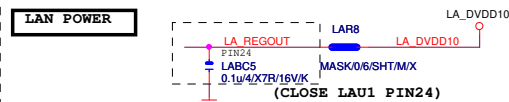
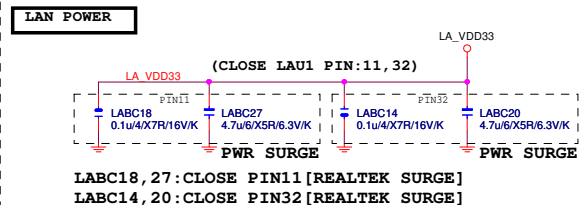
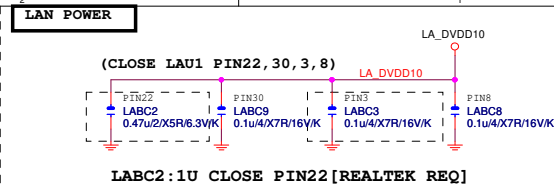
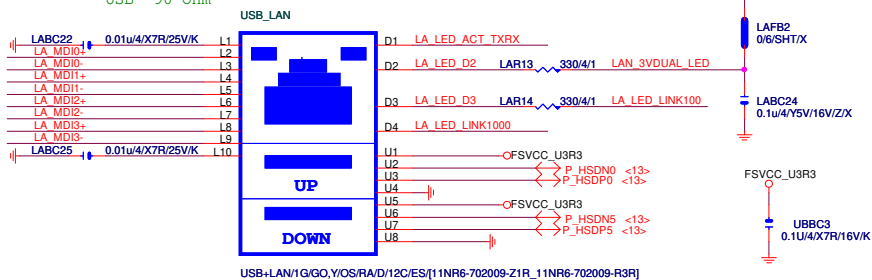
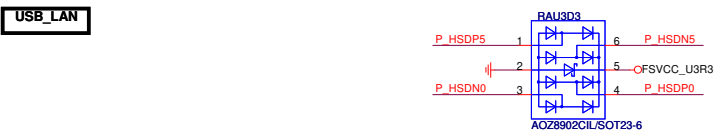
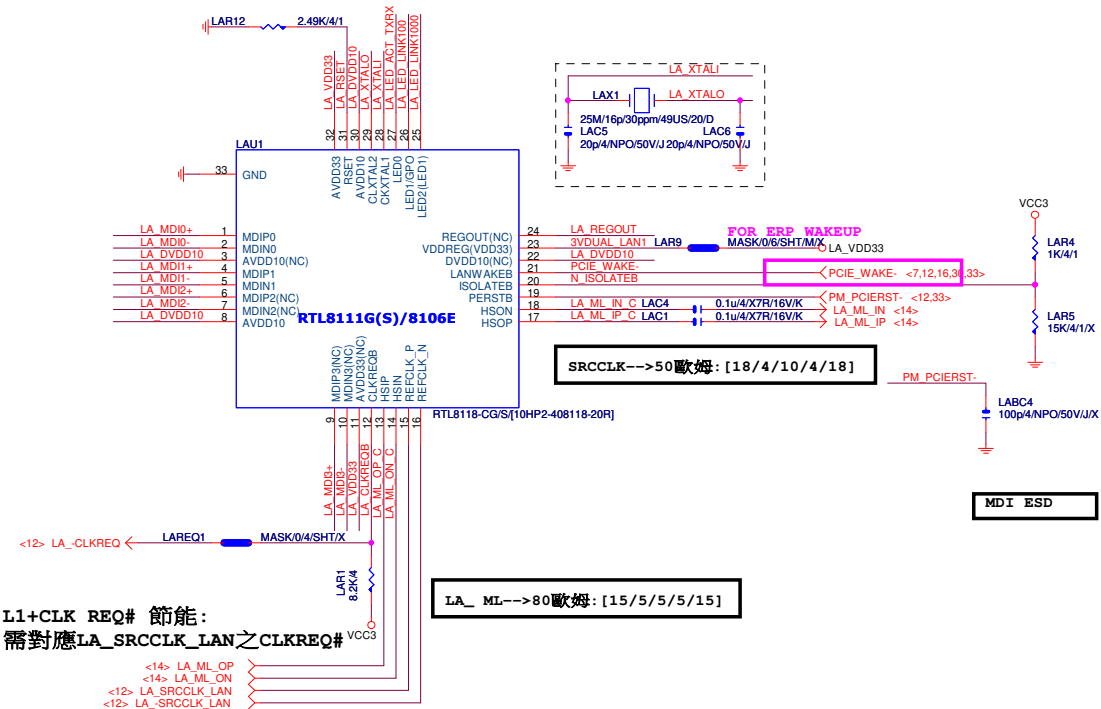


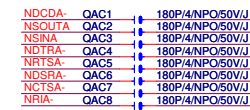
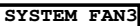
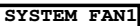
DDRVTT



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Title		
DDR PWR, 5VDUAL, 3VDUAL		
Size	Document Number	Rev
Custom	B450 AORUS ELITE V2	1.01
Date:	Wednesday, August 12, 2020	Sheet 28 of 39





Date: Wednesday, August 12, 2020 Sheet 30 of 39



GIGABYTE™		
Title DP to VGA		
Size Custom	Document Number B450 AORUS ELITE V2	Rev 1.01
Date: Wednesday, August 12, 2020	Sheet 1	of 31

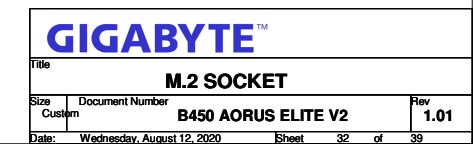
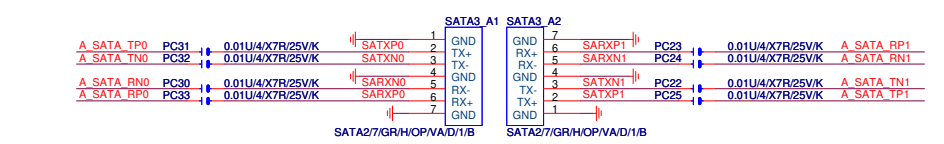
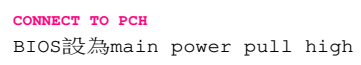
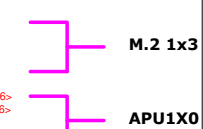
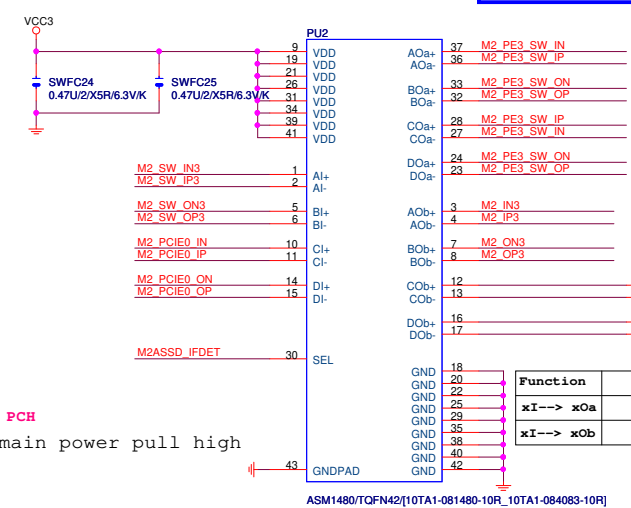
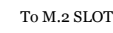
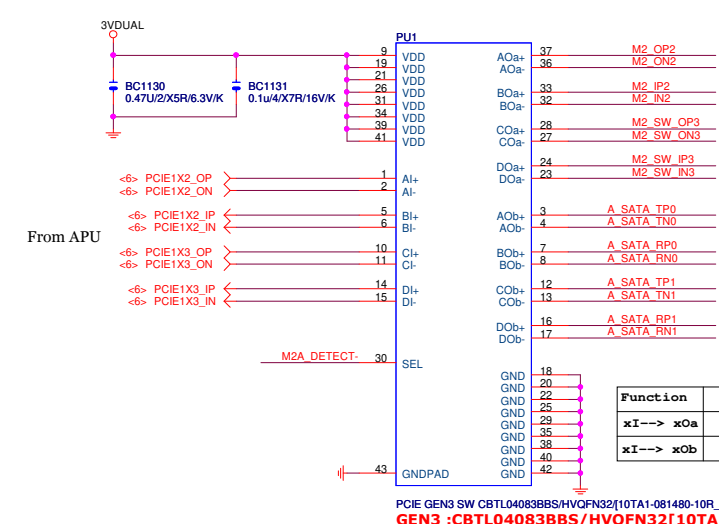
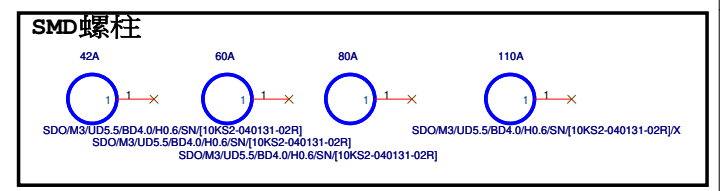
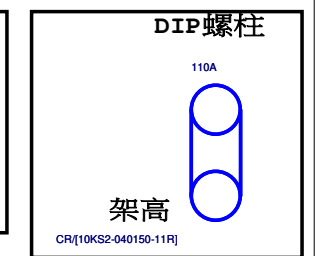
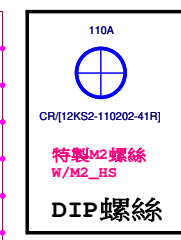
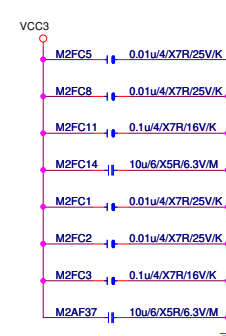
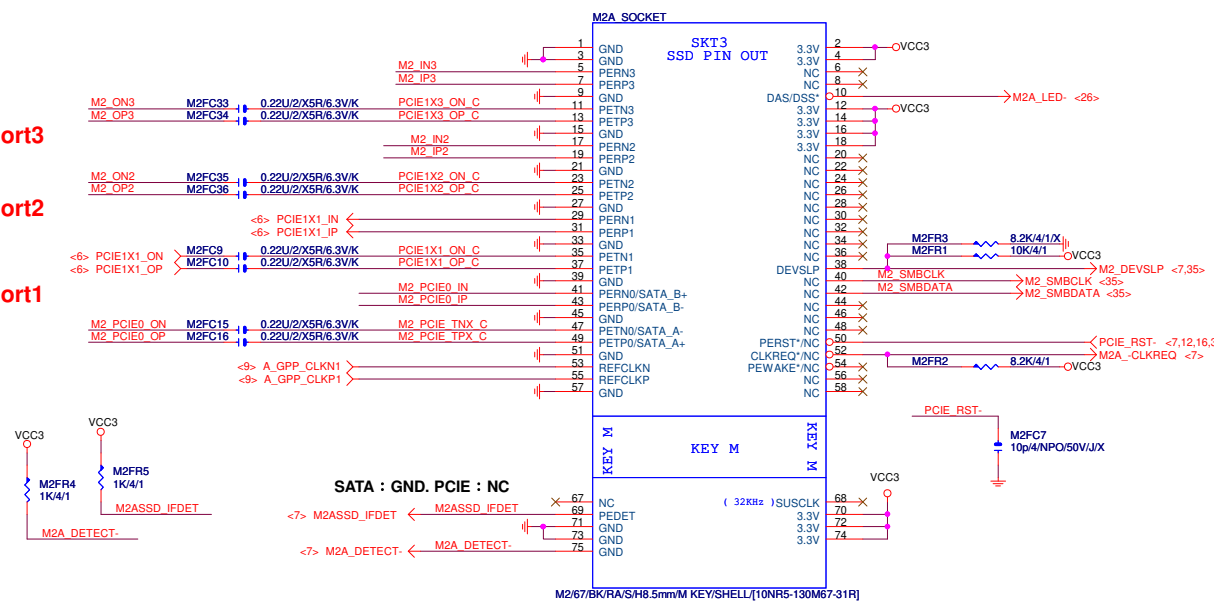
Rev 0.5

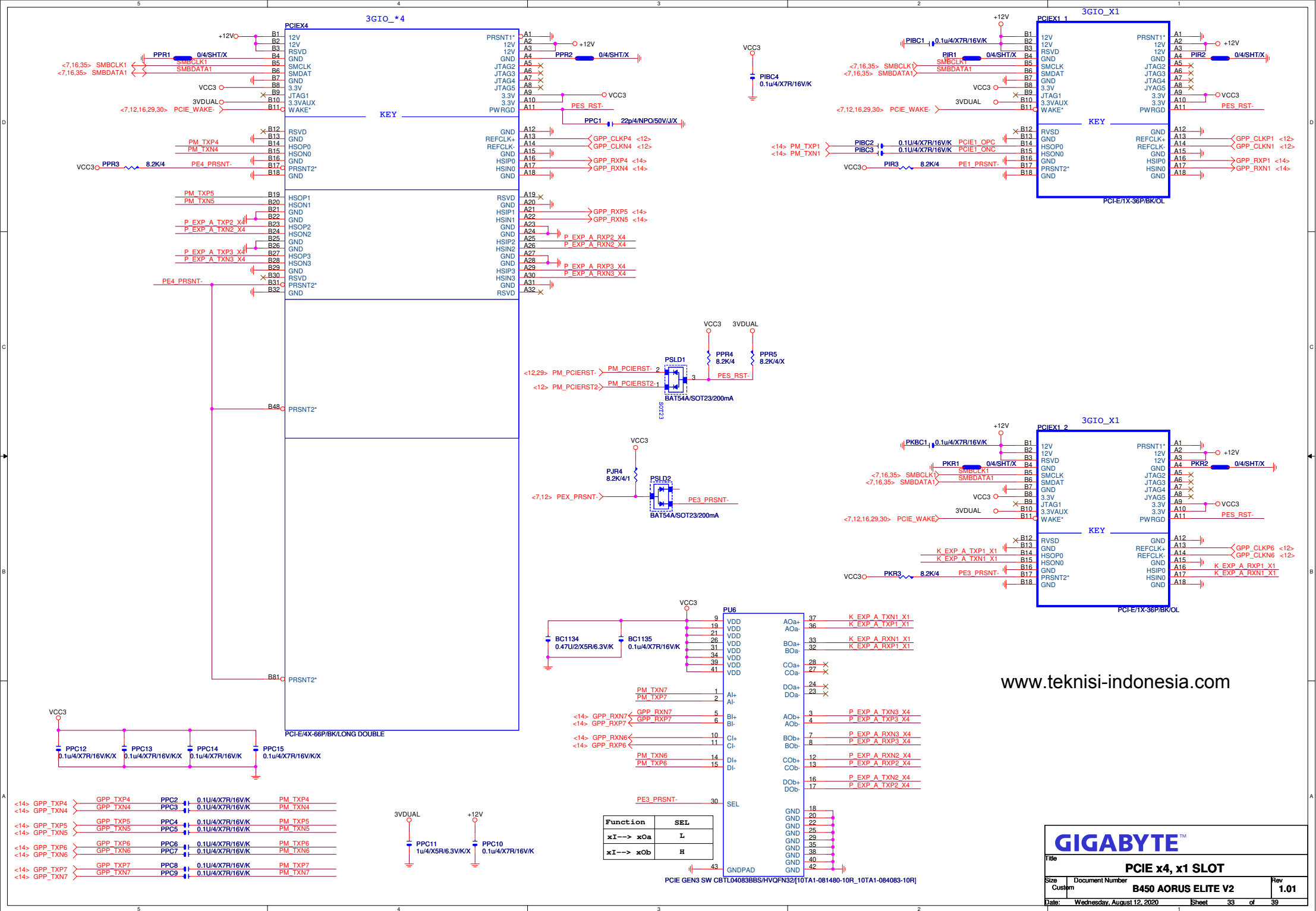
M.2 Lane4 from AM4 port3

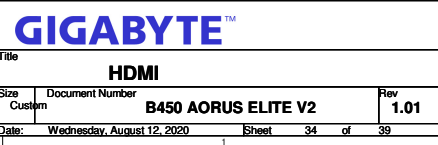
M.2 Lane4 from AM4 port2

M.2 Lane4 from AM4 port1

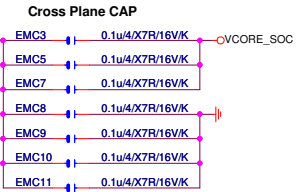
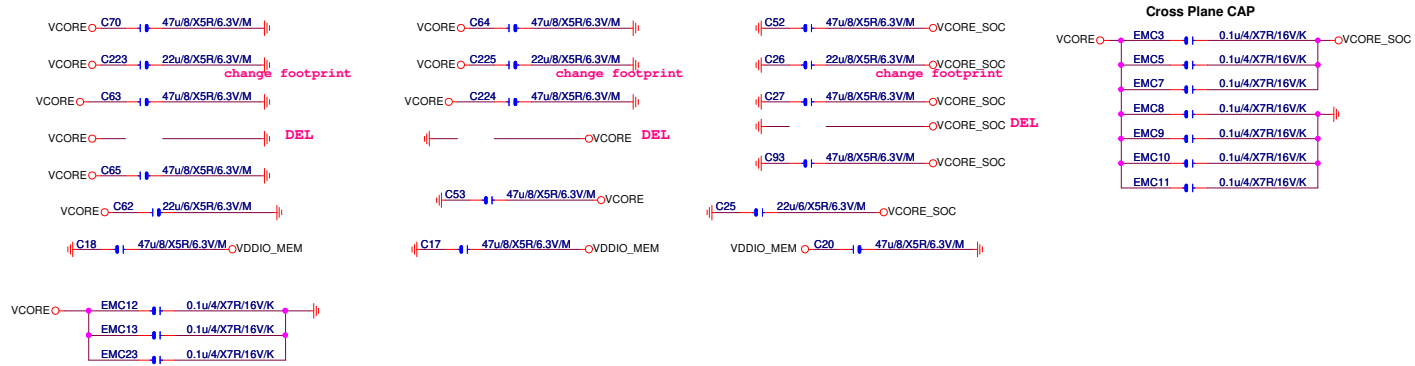
by SWITCH Select



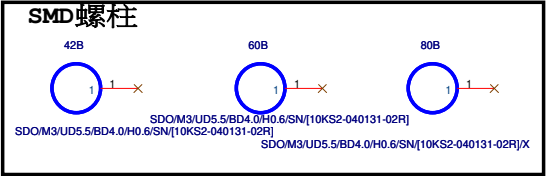
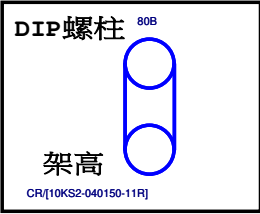
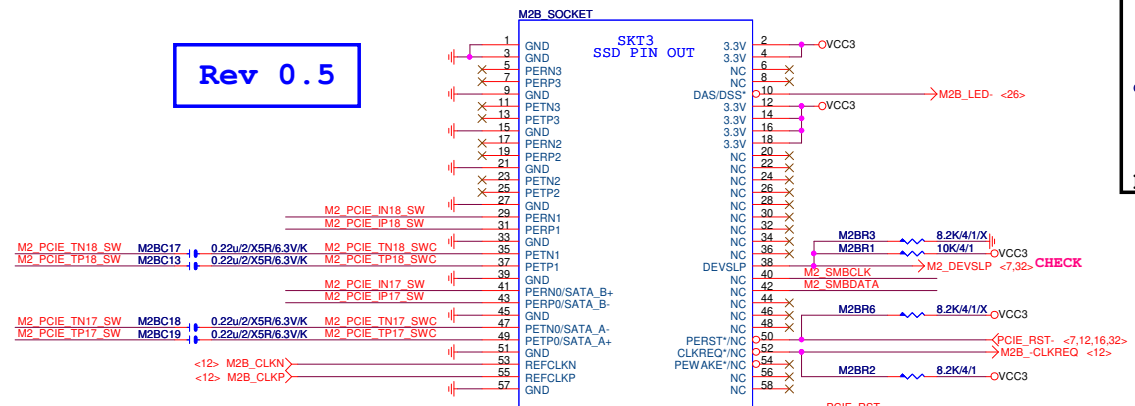




CPU TOP CAVITY

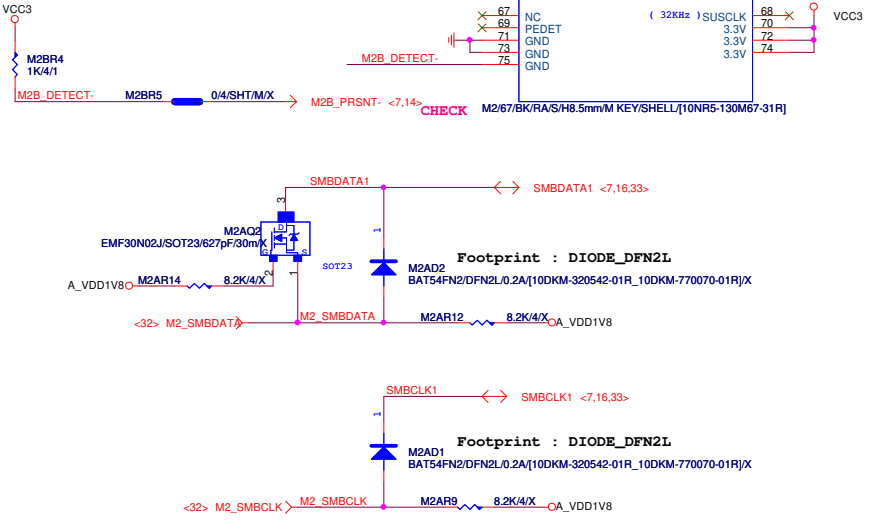


Rev 0.5



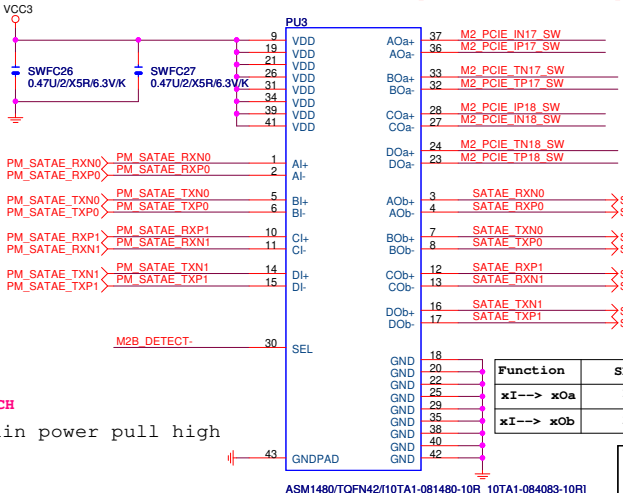
M2 HEATSINK

支援 M.2 function only



From PM SATAE

CONNECT TO PCH
BIOS設為main power pull high



To M.2B PCIE Mode

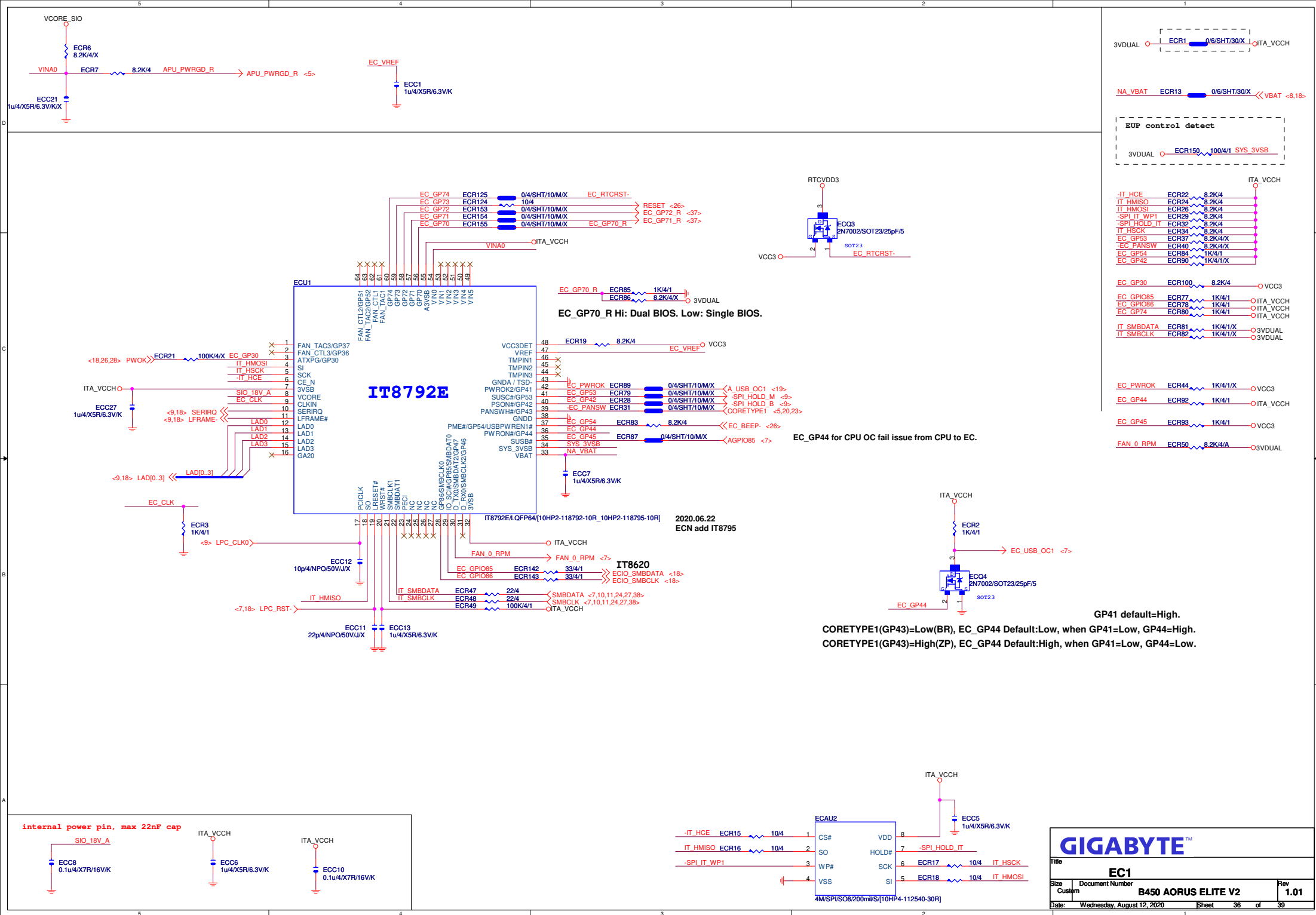
To SATA CONN

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Title: **HDMI**

Size: Custom Document Number: **B450 AORUS ELITE V2** Rev: **1.01**

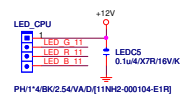
Date: Wednesday, August 12, 2020 Sheet: 35 of 39



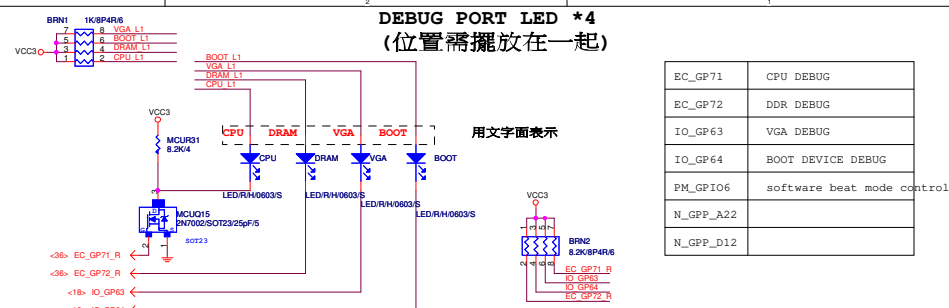
第一區 LED

FOR CPU 正發光 LED*4
(在CPU CHOKE之間,MOS_HS下方,不外露)

AMD CPU_FAN LED connector



DEBUG PORT LED *4
(位置需擺放在一起)



EC_GP71	CPU DEBUG
EC_GP72	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEVICE DEBUG
PM_GPIO6	software beat mode control
N_GPP_A22	
N_GPP_D12	

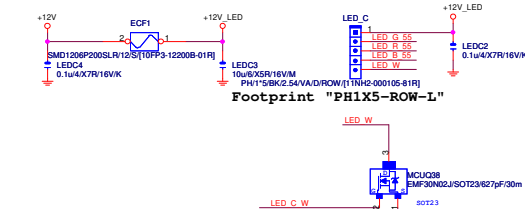
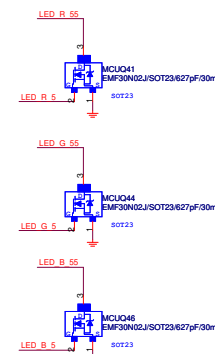
第二區 LED

FOR DIMM 側發光 LED*12
(位置在DIMM兩側)

第五區 LED

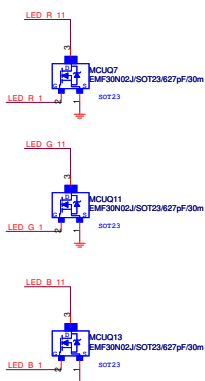
燈條 LED (LED_C1放在PCB左邊板邊位置)

第五區 LED CONTROL

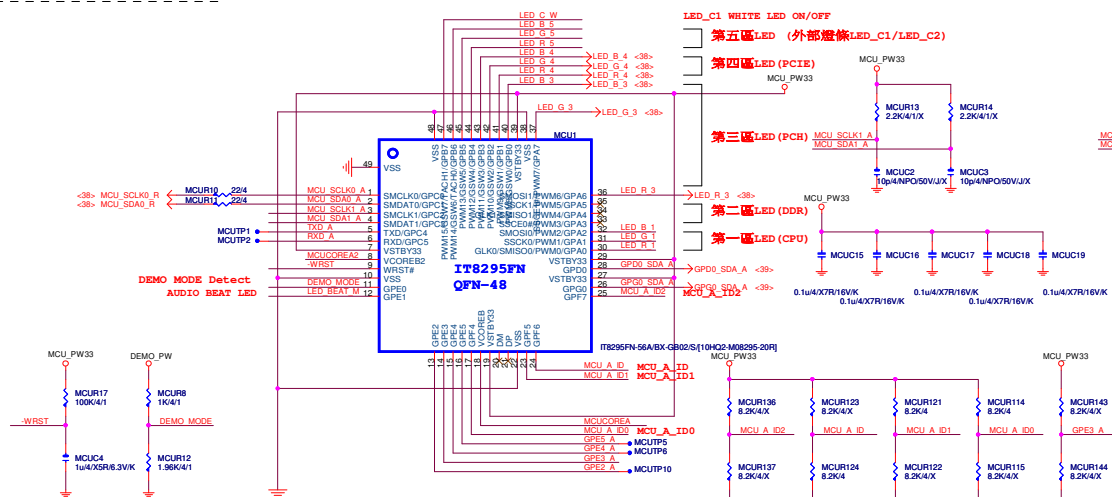
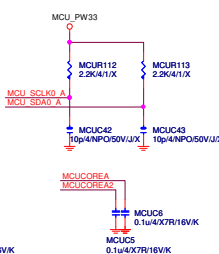
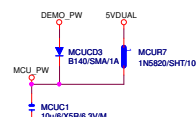
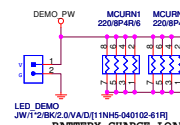
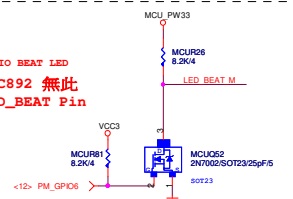


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第一區 LED CONTROL

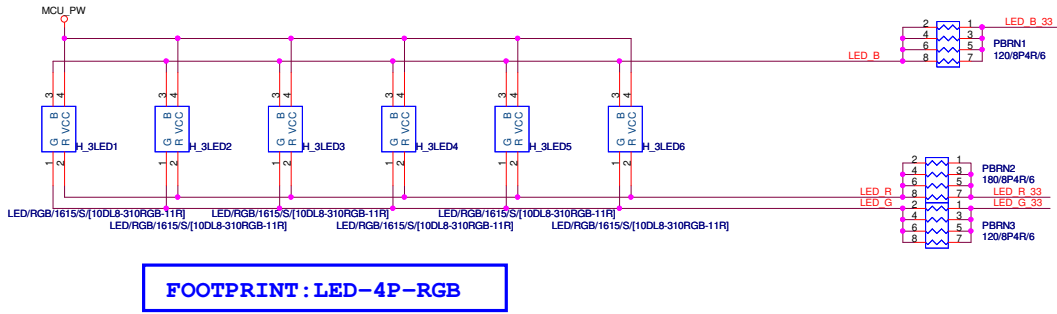


AUDIO BEAT LED
ALC892 無此
LED_BEAT Pin

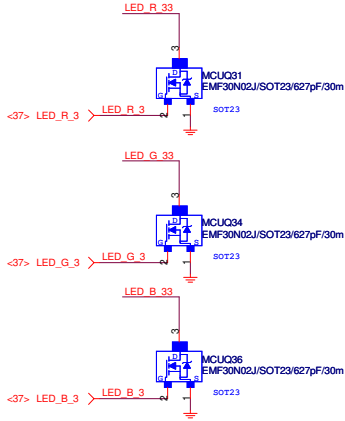


第三區 LED

FOR PCH 正發光 LED*6 (位置在正板,依據PCH_HS設計擺放)

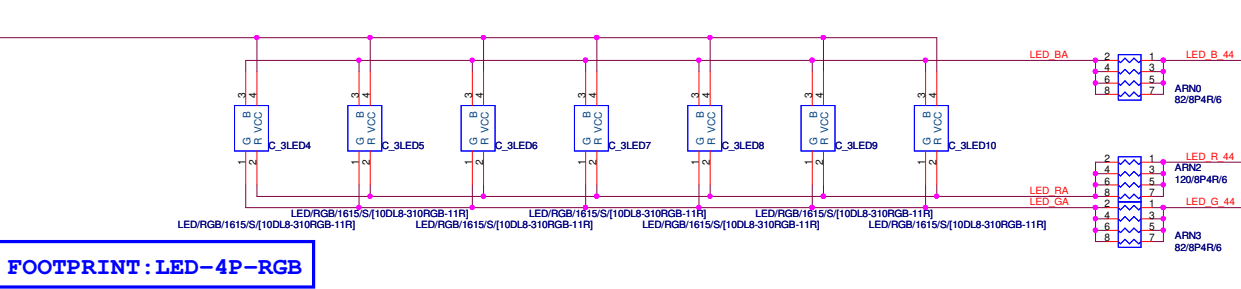


第三區 LED CONTROL

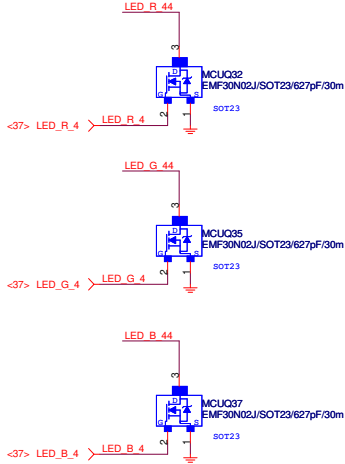


第四區 LED

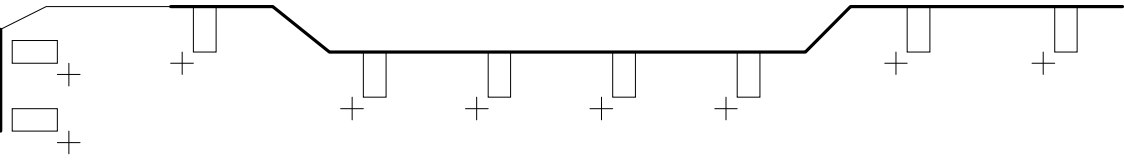
FOR AUDIO 正發光 LED*10 C_3LED1~10)



第四區 LED CONTROL



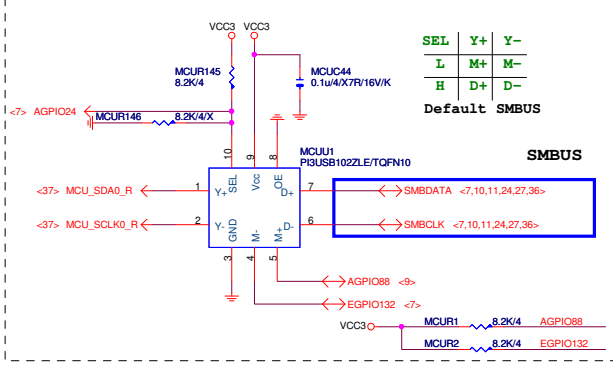
Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項 :

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1, ECF2, ECF3, ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B, GPD0_SDA_BB, GPD0_SDA_C, GPD0_SDA_CC

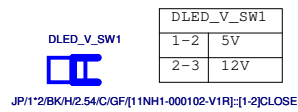
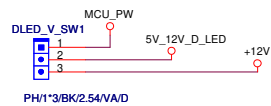
For AMD MCU update



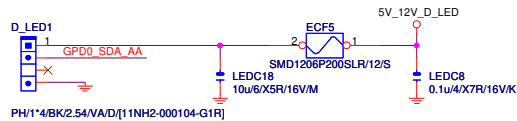
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File		
PCH/AUDIO LED		
Size	Document Number	Rev
Custom	B450 AORUS ELITE V2	1.01
Date: Wednesday, August 12, 2020 Sheet 38 of 39		

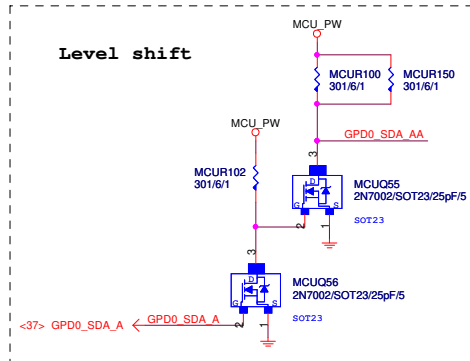
第六區 LED (靠近左上板邊位置)



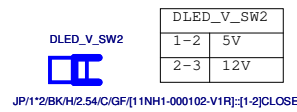
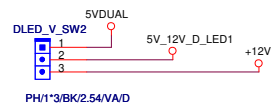
Digital LED Strip1



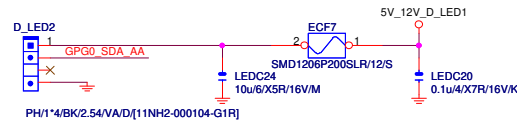
Footprint "PH1X4-CUT3-LED-L"



第七區 LED (靠近右下DDR板邊位置)



Digital LED Strip2



Footprint "PH1X4-CUT3-LED-L"
(for pin-name 與 model-name 同方向)

